INFORMATICS COMPUTATIONAL SCIENCES

MOHANLAL SUKHADIA UNIVERSITY, UDAIPUR-313002

BCA IST SEMESTER-2011

BCA-S104-COMPUTER ORGANIZATION

MODEL PAPER

MARKS: 45 **TIME: 1 ½ hr.**

PART-A

Attempt all the questions. All Questions carry 1 Marks each.

Q.1 The first person who published paper on using computers to perform tasks Other than computations is

a. Charles Babbage
b. Lady Lovelace
c. Alan Turing
d. Konrad Zuse

Q.2 what was the name of the government funded computer used during World War II to compute firing tables?

a. VAX computer
b. IBM computer
c. Colossus computer
d. ENIAC computer

Q.3 which of the following statement is not by ohm's law?

a. I α V
b. I α I / R
c. I α R
d. none of these

Q.4 A resistor with a nominal value of 2.7 KΩ±10% is used in a cassette recorder
Its colorcode is:

a. red,violet,red and silver
b. red,violet,orange and silver
c. red,violet,yellow and gold
d. red,violet,red and gold

Q.5 which of the following capacitors can have the highest capacitance value:

a. Mica b. Paper c. ceramic d. electrolytic

Q.6 asynchronous counter is called:

a. clock pulses receive same time
b. clock pulses receive different time
c. clock pulses receive any time
d. different clock pulses receive different time.

Q.7 the charge on a hole is:

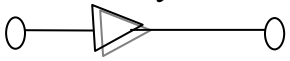
a. 1.6×10^{-9} coulomb
b. 1.6×10^{-8} coulomb
c. 1.6×10^{-12} coulomb
d. 1.6 coulomb

Q.8 the resistance of the diode is equal to:

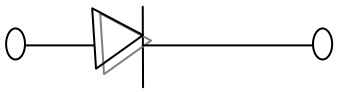
a. ohmic resistance of the P- and N semiconductor
b. junction resistance
c. reverse resistance
d. algebraic sum of a & b

Q.9 the schematic symbol for a PN-Junction diode is:

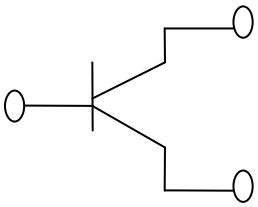
a.



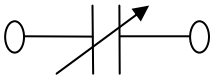
b.



c.



d .



Q.10 which of the logic families is well suited for high speed operation?

a. TTL b. ECL c. CMOS d. RTL

Q.11 the donar type impurities:

a. creat excess holes.

b. can be added to Ge but not Si

c. must have only three valance e^-

D must have only five valance e^-

Q.12 In order to execute program instructions must be transferred from memory along a bus to the CPU. If the bus has 8 data lines, at most one 8 bit byte can be transferred at a time. How much memory access would be needed in this case to transfer a 32 bit instruction from memory to the CPU?

a. 1 b. 2 c. 3 d. 4

Q.13 Interrupts can be generated in response to

a. detected program errors such as arithmetic overflow or division by zero
b. detected hardware faults
c. Input/output activities
d. Internal timers
e. b, c, and d
f. a, b, c, and d

Q.14 The ALU and control unit of most of the microcomputers are Combined and manufacture on a Single silicon chip. What is it called?

a. monochip
b. microprocessor
c. ALU
d. control unit

Q.15 What is the control unit's function in the CPU?

a. To transfer data to primary storage
b. to store program instruction
c. to perform logic operations
d. to decode program instruction

Q.16 CPU does not perform the operation

a. data transfer
b. logic operation
c. arithmetic operation
d. all of above

Q.17 the speed imbalance between memory access and CPU operation can be Reduced by:

a. cache memory
b. memory inter leaving
c. reducing the size of memory
d. none of the above

Q.18 the sequence of events that happen during typical fetch operations is:

a. PC----MAR---MEMORY----MDR----IR
b. PC---MEMORY----MDR----IR
c. PC---MEMORY----IR
d. PC---MAR----MEMORY----IR

Q.19 any instruction should have at least:

a. 2 operand **b**. 1 operand **c.** 3 operand **d.** none of the above

Q.20 the three main component of a digital computer system are:

a. memory, I/O,DMA
b. ALU, CPU, memory
c. memory,CPU,I/O
d. control circuits,ALU,registers

Q.21 which of the following instruction will never affect the zero flag?

a. DCR registers b. ORA register c. DCX register d. XRA register

Q.22 the instruction used to shift registers the accumulator contents by one bit Through the carry Flag bit is:

a. RLC b. RAL c. RRC d. RAR

Q.23 a computer's memory is composed of 8K words of 32 bits each. How many bits are required for memory address if the smallest addressable memory unit is a word?

a. 13 b. 8 c. 10 d. 6

Q.24 a given memory chip has 12 address pins and 4 data pins. It has the Following number of Locations.

a. 2^4 b. 2^{12} c. 2^{48} d. 2^{16}

Q.25 How many address lines are needed to address each memory locations in a 2048 x 4 memories Chip?

a. 10 b. 11 c. 8 d. 12

Q.26 In immediate addressing the operand is placed

a. in the CPU register

b. after OP code in the instruction

c. in memory

d. in stack

Q.27 the most common addressing techniques employed by a CPU is

a. immediate b. direct c. indirect d. register e. all of the above

Q.28 Pipeline implement

a. fetch instruction b. decode instruction c. fetch operand

d. calculate operand e. execute instruction f. all of above

Q.29 A stack pointer is :

a. a 16-bit register in the microprocessor that indicate the beginning of the stack memory.
b. a register that decodes and executes 16-bit arithmetic expression.
c. The first memory location where a subroutine address is stored.
d. a register in which flag bits are stored

Q.30 which of the following about the program counters PC is true:

a. it is a register b. it is a cell in ROM
c. during execution of the current instruction its content changes
d. none of the above
e a & c
f b & a

Q.31 which of the following are registers:

a. Accumulator b. stacks pointer
c. Program counters d.all of the above e. Buffer

Q.32 the most relevant addressing mode to write position independent code is:

a. direct b. Indirect c. Relative d. Indexed

Q.33 in the indirect addressing scheme the second part of the instruction Contains:

a. the operand is decimal form
b. the address of the location where the value of the operand is stored
c. the address of the location where the address of the operand is stored
d.the operand is an encoded form

Q.34 what characteristic of RAM memory makes it not suitable for permanent storage?

a. too slow
b. unreliable
c. it is volatile
d. too bulky

Q.35 which of the following is non volatile memory:

a. EEPROM b. SRAM c. DRAM d. none of the above

Q.36 ram is called DRAM when:

a. it is always moving around data
b. it requires periodic refreshing
c. it can do several thing simultaneously
d. none of the above

Q.37 a major advantage of direct mapping of a cache is its simplicity. The main Disadvantage of this Organization is that

a. It does not allow simultaneous access to the intended data and its tag
b. It is more expensive than other types of cache organizations
c. The cache hit ratio is degraded if two or more blocks used alternately Map onto the same block frame in the cache
d. Its access time is greater than that of other cache organizations
e. The number of blocks required for the cache increases linearly with the Size of the main Memory.

Q.38 Which of the following is not an advantage of a cache memory?

a. high speed
b. less time
c. less cost
d.None of the above

Q.39 if memory access time takes 20ns with cache and 110ns without it then The hit ratio is:

a. 93% b. 90% c. 87% d.88%

Q.40 every computer must at least consist of:

a. data bus b. address bus c. control bus d. all of the above

Q.41 Microprocessor 8085 can address location upto

a. 32K b. 128K c. 64K d. 1M

Q.42 the first operating system used in microprocessor :

a. ZENIX b. DOS c. CP/M d. MULTICS

Q.43 choose the correct statement :

a. bus Is group of information carriying wire

b. bus it needed to acheive raisonnable speed of opération

c. bus can carry data and adresses

d. a bus can be shared by move than one device

e. all.

Q.44 the 8085 micro processor enters into wait state after the recognition of :

a. HOLD b.*READY c.*RESET-IN d. INTR

Q.45 micro program is :

a. the name of a sourse program in micro computer

b. the set of instruction indicating the primitive operations in a systems.

c. the premitive form of macros use dis assembly language programming

d.a program is very small size