AX131	**Advanced Digital Signal Processing**	**3**	**0**	**0**	**100**

1. DISCRETE RANDOM SIGNAL PROCESSING **9**

Discrete Random Processes, Expectations, Variance, Co -Variance, Scalar Product, Energy of Discrete Signals - Parseval's Theorem, Wiener Khintchine Relation - Power Spectral Density - Periodogram - Sample Autocorrelation - Sum Decomposition Theorem, Spectral Factorization Theorem - Discrete Random Signal Processing by Linear Systems - Simulation of White Noise - Low Pass Filtering of White Noise.

2. SPECTRUM ESTIMATION **9**

Non-Parametric Methods-Correlation Method - Co-Variance Estimator - Performance Analysis of Estimators - Unbiased, Consistent Estimators-Periodogram Estimator-Barlett Spectrum Estimation-Welch Estimation-Model based Approach - AR, MA, ARMA Signal Modeling-Parameter Estimation using Yule-Walker Method.

3. LINEAR ESTIMATION AND PREDICTION **9**

Maximum likelihood criterion-efficiency of estimator-Least mean squared error criterion -Wiener filter-Discrete Wiener Hoff equations-Recursive estimators-Kalman filter-Linear prediction, prediction error-whitening filter, inverse filter-Levinson recursion, Lattice realization, and Levinson recursion algorithm for solving Toeplitz system of equations.

4. ADPATIVE FILTERS **9**

FIR adaptive filters-Newton's steepest descent method - adaptive filter based on steepest descent method-Widrow Hoff LMS adaptive algorithm- Adaptive channel equalization-Adaptive echo chancellor-Adaptive noise cancellation-RLS adaptive filters-Exponentially weighted RLS-sliding window RLS-Simplified IIR LMS adaptive filter.

5. MULTIRATE DIGITAL SIGNAL PROCESSING **9**

Mathematical description of change of sampling rate - Interpolation and Decimation - continuous time model - Direct digital domain approach - Decimation by an integer factor - Interpolation by an integer factor - Single and multistage realization - poly phase realization - Application to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals.

Total No of periods: 45

AX131 Advanced Digital Signal Processing **3** **0** **0** **100**

Text Book:

1. Monson H.Hayes, " Statistical Digital Signal Processing and Modeling ", John Wiley and Sons, Inc., New York, 1996.

References:

1. Sopocles J.Orfanidis, " Optimum Signal Processing ", McGraw Hill, 1990.
2. John G.Proakis, Dimitris G.Manolakis, " Digital Signal Processing ", Prentice Hall of India, 1995.

AX132	**Introduction to VLSI Design**	**3**	**0**	**0**	**100**

1. MOS TECHNOLOGY AND CIRCUITS 9

MOS Technology and VLSI, Process parameters and considerations for BJT, MOS and CMOS, Electrical properties of MOS circuits and Device modeling.

2. MOS CIRCUIT DESIGN PROCESS 9

MOS Layers, Stick diagram, Layout diagram, Propagation delays, Examples of combinational logic design, Scaling of MOS circuits.

3. DIGITAL CIRCUITS AND SYSTEMS 9

Programmable Logic Array (PLA) and Finite State Machines, Design of ALUs, Memories and Registers.

4. ANALOG VLSI AND HIGH SPEED VLSI 9

Introduction to Analog VLSI, Realisation of Neural Networks and Switched capacitor filters, Sub-micron technology and GaAs VLSI technology.

5. HARDWARE DESCRIPTION LANGUAGES 9

VHDL background and basic concepts, Structural specifications of hardware design organisation and parametrisation.

Total No of periods: 45

AX132 Introduction to VLSI Design **3 0 0 100**

References:

1. *Douglas A. Pucknell and Kamran Eshraghian, " Basic VLSI Design Systems and Circuits ", Prentice Hall of India Pvt Ltd., 1993.*
2. *Wayne Wolf , " Modern VLSI Design ", 2nd Edition, Prentice Hall,1998.*
3. *Amar Mukherjee, " Introduction to NMOS and CMOS VLSI System Design ", Prentice Hall, 1986.*
4. *Randall .L.Geiger and P.E. Allen, " VLSI Design Techniques for Analog and Digital Circuits ", McGraw-Hill International Company, 1990.*
5. *Fabricious. E , " Introduction to VLSI Design ", McGraw Hill, 1990.*
6. *Navabi .Z., " VHDL Analysis and Modeling of Digital Systems ", McGraw Hill, 1993.*
7. *Mohmmed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", McGraw-Hill, 1994.*
8. *Peter J. Ashenden, " The Designer's Guide to VHDL ", Harcourt Asia Private Limited & Morgan Kauffman, 1996.*

AX133 Advanced Digital System Design **3 0 0 100**

1. ADVANCED TOPICS IN BOOLEAN ALGEBRA **9**

Shannon's expansion theorem, Conseusus theorem, Octal designation, Run measure, INHIBIT / INCLUSION / AOI / Driver / Buffer gates, Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.

2. THRESHOLD LOGIC **9**

Linear seperability, Unateness, Physical implementation, Dual comparability, Reduced functions, Various theorems in threshold logic, Synthesis of single gate and multigate threshold Network.

3. SYMMETRIC FUNCTIONS **9**

Elementary symmetric functions, Partially symmetric and totally symmetric functions, Mc Cluskey decomposition method, Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.

4. SEQUENTIAL LOGIC CIRCUITS **9**

Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards Unger's theorem.

5. PROGRAMMABLE LOGIC DEVICES **9**

Basic concepts, Programming technologies, Programmable Logic Element (PLE), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Structure of Standard PLD's, Complex PLD's (CPLD).
System Design Using PLD's - Design of combinational and sequential circuits using PLD's, Programming PAL device using PALASM, Design of state machine using Algorithmic State Machines (ASM) chart as a design tool.
Introduction To Field Programmable Gate Arrays - Types of FPGA, Xilinx XC3000 series, Logic Cell array (LCA), Configurable Logic Blocks (CLB) Input/Output Block (IOB)- Programmable Interconnect Point (PIP), Introduction to Actel ACT2 family and Xilinx XC4000 families, Design examples.

Total No of periods: 45

References:

1. William I. Fletcher, " An Engineering Approach to Digital Design " , Prentice Hall of India, 1996.
2. James E. Palmer, David E. Perlman, " Introduction to Digital Systems ", Tata McGraw Hill, 1996.
3. N.N. Biswas, " Logic Design Theory ", Prentice Hall of India, 1993.
4. S. Devadas, A. Ghosh and K. Keutzer, " Logic Synthesis ", Mc Graw Hill, 1994.

MA151	**Applied Mathematics for Electronics Engineers**	**3**	**1**	**0**	**100**

1. THE WAVE EQUATIONS **10**

Solution of initial and boundary value problems- Characteristics- D'Alembert's Solution - Significance of characteristic curves - Laplace transform solutions for displacement in a long string- a long string under its weight - a bar with prescribed force on one end- free vibrations of a string.

2. SPECIAL FUNCTIONS **13**

Series solutions- Bessel's equation - Bessel Functions-Legendre's equation - Legendre polynomials - Rodrigue's formula - Recurrence relations- generating functions and orthogonal property for Bessel functions of the first kind - Legendre polynomials.

3. PROBABILITY AND RANDOM VARIABLES **12**

Probability Concepts -Random Variables, Moment generating function - standard distributions- Two dimensional random variables- Transformation of Random Variables - Correlation - Regression system - queueing applications.

4. QUEUEING THEORY **10**

Single and Multiple server Markovian queueing models - customer impatience - Priority queues - M/G/1 queueing system - queueing applications.

5. TUTORIALS **15**

Total No of periods: 60

MA151 Applied Mathematics for Electronics Engineers 3 1 0 100

References:

1. Sankara Rao.K. " Introduction to Partial Differential Equation ", PHI, 1995.
2. Taha. H.A., " Operations Research- An Introduction " 6th Edition, PHI, 1997.
3. Churchil. R.V., " Operational Mathematics ", McGraw Hill, 1972.
4. Richard A.Johnson, Miller and Freund's Probability and Statistics for Engineers, 5th Edition, PHI, 1994.
5. S.Narayanan, T.K.Manickvachagam Pillay and G.Ramanaiah - " Advanced Mathematics for Engineering Students " Vol.II, S.Viswanathan Pvt. Ltd., 1986.

VL132 Solid State Device Modeling and Simulation **3 0 0 100**

1. BASIC SEMICONDUCTOR PHYSICS **7**

Quantum Mechanical Concepts, Carrier Concentration, Transport Equation Bandgap, Mobility and Resistivity, Carrier Generation and Recombination, Avalanche Process, Noise Sources.

2. MODELING BIPOLAR DEVICE PHENOMENA **10**

Injection and Transport Model, Continuity Equation, Diode Small Signal and Large Signal (Change Control Model), Transistor Models: Ebber - Molls and Gummel Port Model, Mextram model, SPICE modeling temperature and area effects.

3. MOSFET MODELING **10**

Introduction Interior Layer, MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

4. PARAMETER MEASUREMENT **10**

General Methods, Specific Bipolar Measurement, Depletion Capacitance, Series Resistances, Early Effect, Gummel Plots, MOSFET: Long and Short Channel Parameters, Statistical Modeling of Biopolar and MOS Transistors.

5. OPTOELECTRONIC DEVICE MODELS **8**

Static and Dynamic Models, Rate Equations, Numerical Technique, Equivalent Circuits, Modeling of LEDs, Laser Diode and Photo Detectors.

Total No of periods: 45

VL132 Solid State Device Modeling and Simulation 3 0 0 100

Text Books:

1. *Philip E. Allen, Douglas R.Hoberg, " CMOS Analog Circuit Design " Second Edition, Oxford Press-2002 (Unit III).*
2. *CMOS / BiCMOS CLSI Low Voltage Power Kiat Seng Yeo, Samir S.Rofail, Wang-Ling Gob, Person education low price edition 2002 (Unit IV).*

References:

1. *S.M.Sze " Semiconductor Devices - Physics and Technology ", John Wiley and sons 1985 (Unit I, Unit II).*
2. *Giuseppe Massobrio and Paolo Antogentti, " Semiconductor Device Modeling with SPICE " Second Edition, McGraw-Hill Inc, New York, 1993. (Unit I, Unit II and Unit III).*
3. *Mohammed Ismail & Terri Fiez " Analog VLSI-Signal & Information Processing ", (Statistical modeling of MOSFET unit IV).*

AX134 Analysis and Design of Analog Integrated Circuits 3 0 0 100

1. CIRCUIT CONFIGURATION FOR LINEAR IC 9

Current sources, analysis of difference amplifiers with active load, supply and temperature independent biasing techniques, voltage references.

2. OPERATIONAL AMPLIFIERS 9

Analysis of Operational amplifier circuits, slew rate model and high frequency analysis, operational amplifier noise analysis and low noise operational amplifiers.

3. ANALOG MULTIPLIER AND PLL 9

Analysis of four quadrant and variable transconductance multiplier, voltage controlled oscillator, closed loop analysis of PLL.

4. MOS ANALOG ICS 9

Design of MOS Operational Amplifier, CMOS voltage references, MOS Power amplifier and analog switches.

5. MOS SWITCHED CAPACITOR FILTERS 9

Design techniques for switched capacitor filter, CMOS switched capacitor filters, MOS integrated active RC Filters.

Total No of periods: 45

AX134 Analysis and Design of Analog Integrated Circuits 3 0 0 100

References:

1. Gray and Meyer, " Analysis and Design of Analog ICs ", Wiley International, 1996.
2. Gray, Wooley, Brodersen, " Analog MOS Integrated Circuits ", IEEE Press, 1989.
3. Kenneth R. Laker, Willy M.C. Sansen, William M.C.Sansen, " Design of Analog Integrated Circuits and Systems ", McGraw Hill, 1994.
4. Behzad Razavi, " Principles of Data Conversion System Design ", S. Chand & Company Ltd, 2000.

AX141 Computer Architecture and Parallel Processing **3 0 0 100**

1. THEORY OF PARALLELISM **15**

Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties - Conditions of parallelism, Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance - performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

2. HARDWARE TECHNOLOGIES **10**

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory - backplane bus systems, cache memory organisations, shared memory organisations, sequential and weak consistency models.

3. PIPELINING AND SUPERSCLAR TECHNOLOGIES **10**

Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

4. SOFTWARE AND PARALLEL PROGRAMMING **10**

Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

Total No of periods: 45

References:

1. *Kai Hwang, " Advanced Computer Architecture ", McGraw Hill International, 1993.*
2. *William Stallings, " Computer Organization and Architecture ", Macmillan Publishing Company, 1990.*
3. *M.J. Quinn, " Designing Efficient Algorithms for Parallel Computers ", McGraw Hill International, 1994.*

AX143 Embedded Systems	3	0	0	100

1. INTRODUCTION REVIEW OF EMBEDDED HARDWARE 9

Terminology Gates - Timing Diagram - Memory - microprocessors Buses-Direct Memory Access-interrupts - Built-ins on the Microprocessor-Conventions Used on Schematic-schematic. Interrupts Microprocessor Architecture-Interrupt Basics-Shared Data Problem-Interrupt latency.

2. PIC MICROCONTROLLER AND INTERFACING 9

Introduction, CPU architecture, registers, instruction sets addressing modes Loop timing, timers, Interrupts, Interrupt timing, I/o Expansion, I 2C Bus Operation Serial EEPROM, Analog to digital converter, UART-Baud Rate-Data Handling-Initialisation, Special Features - serial Programming-Parallel Slave Port.

3. EMBEDDED MICROCOMPUTER SYSTEMS 9

Motorola MC68H11 Family Architecture Registers, Addressing modes Programs. Interfacing methods parallel I/o interface, Parallel Port interfaces, Memory Interfacing, High Speed I/o Interfacing, Interrupts-interrupt service routine-features of interrupts-Interrupt vector and Priority, timing generation and measurements, Input capture, Output compare, Frequency Measurement, Serial I/o devices Rs.232, Rs.485. Analog Interfacing, Applications.

4. SOFTWARE DEVELOPMENT AND TOOLS 9

Embedded system evolution trends. Round - Robin, robin with Interrupts, function-One-Scheduling Architecture, Algorithms. Introduction to-assembler-compiler-cross compilers and Intergrated Development Environment (IDE). Object Oriented Interfacing, Recursion, Debugging strategies, Simulators.

5. REAL TIME OPERATING SYSTEMS 9

Task and Task States, tasks and data, semaphores and shared Data Operating system Services-Message queues-Timer Function-Events-Memory Management, Interrupt Routines in an RTOS environment, basic design Using RTOS.

Total No of periods: 45

AX143 Embedded Systems **3 0 0 100**

Text Books:

1. *David E Simon, " An embedded software primer ", Pearson education Asia, 2001.*
2. *John B Peat man " Design with Microcontroller ", Pearson education Asia, 1998.*
3. *Jonartthan W. Valvano Brooks/cole " Embedded Micro computer Systems. Real time Interfacing ", Thomson learning 2001.*

References:

1. *Burns, Alan and Wellings, Andy, " Real-Time Systems and Programming Languages ", Second Edition. Harlow: Addison-Wesley-Longman, 1997.*
2. *Raymond J.A. Bhur and Donald L.Bialey, " An Introduction to real time systems: Design to networking with C/C++ ", Prentice Hall Inc. New Jersey, 1999.*
3. *Grehan Moore, and Cyliax, " Real time Programming: A guide to 32 Bit Embedded Development. Reading " Addison-Wesley-Longman, 1998.*
4. *Heath, Steve, " Embedded Systems Design ", Newnes 1997.*

VL141	**Computer Aided Design of VLSI Circuits**	**3**	**0**	**0**	**100**

1. **9**

Introduction to VLSI Methodologies - VLSI Physical Design Automation - Design and Fabrication of VLSI Devices - Fabriction process and its impact on Physical Design.

2. **9**

A Quick Tour of VLSI Design Automation Tools - Data structures and Basic Alogrithms - Algorithmic Graph theory and compuittional complexity - Tractable and Intractable problems.

3. **9**

General purpose methods for combinational optimization - partitioning - floor planning and pin assignment - placement - routing.

4. **9**

Simulation-logic synthesis -Verification-High level synthesis- Compaction.

5. **9**

Physcial Design Automation of FPGAs,MCMS-VHDL-Verilog-Implementation of Simple cirucuits using VHDL and Verilog.

Total No of periods: 45

VL141	**Computer Aided Design of VLSI Circuits**	**3**	**0**	**0**	**100**

Text Books:

1. N.A. Sherwani, " Algorithms for VLSI Physical Design Automation ", 1999.
2. S.H.Gerez, " Algorithms for VLSI Design Automation ", 1998.

AX031 ASIC Design **3 0 0 100**

1. INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN **9**

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort - Library cell design - Library architecture .

2. PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS **9**

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA - Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

3. PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY **9**

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX - Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools - EDIF- CFI design representation.

4. LOGIC SYNTHESIS, SIMULATION AND TESTING **9**

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

5. ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING **9**

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow - global routing - detailed routing - special routing - circuit extraction - DRC.

Total No of periods: 45

AX031 ASIC Design **3 0 0 100**

Text Book:

1. M.J.S .Smith, - " Application - Specific Integrated Circuits " - Addison -Wesley Longman Inc., 1997.

References:

1. Andrew Brown, - " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991.
2. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, " Field Programmable Gate Arrays " - Kluever Academic Publishers, 1992.
3. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
4. S. Y. Kung, H. J. Whilo House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

AX033 Neural Networks and its Applications **3 0 0 100**

1. INTRODUCTION TO ARTIFICIAL NEURAL NETWORKS **9**

Neuro-physiology - General Processing Element - ADALINE - LMS learning rule - MADALINE - MR2 training algorithm.

2. BPN AND BAM **9**

Back Propagation Network - updating of output and hidden layer weights -application of BPN - associative memory - Bi-directional Associative Memory - Hopfield memory - traveling sales man problem.

3. SIMULATED ANNEALING AND CPN **9**

Annealing, Boltzmann machine - learning - application - Counter Propagation network - architecture - training - Applications.

4. SOM AND ART **9**

Self organizing map - learning algorithm - feature map classifier - applications - architecture of Adaptive Resonance Theory - pattern matching in ART network.

5. NEOCOGNITRON **9**

Architecture of Neocognitron - Data processing and performance of architecture of spacio - temporal networks for speech recognition.

Total No of periods: 45

AX033 Neural Networks and its Applications **3** **0** **0** **100**

References:

1. *J.A. Freeman and B.M.Skapura , "Neural Networks, Algorithms Applications and Programming Techniques", Addison-Wesely, 1990.*
2. *Laurene Fausett, "Fundamentals of Neural Networks: Architecture, Algorithms and Applications", Prentice Hall, 1994*

AX036 Reliability Engineering **3 0 0 100**

1. INTRODUCTION **9**

Reliability fundamentals and bath tub curve, Reliability measures and parameters, Electronic system reliability, Hazard rate model, Probability concepts and failure time distribution.

2. SYSTEM RELIABILITY **9**

System reliability modeling, v-out of 'n' system, Analysis of complex reliability structures, System reliability estimation.

3. DEVICE RELIABILITY **9**

Accelerated life testing, Early life reliability, Long term device reliability, Electrostatic discharge, Electrical stress, Steady state hazard rate.

4. RELIABILITY TECHNIQUES **9**

Reliability prediction, Cut set, Tie set, FME set, PTA, Markov, Monte Carlo Simulation, Application to electronic systems.

5. MAINTAINABILITY AND AVAILABILITY CONCEPTS **9**

Guidelines for design for maintainability, MITR, BIT / BITE facility, Spares provisioning, Electronics system packaging and interconnections.

Total No of periods: 45

AX036 Reliability Engineering **3 0 0 100**

References:

1. *David J. Klinger, Yoshinao Nakada and Maria A. Menendez, " AT & T Reliability Manual ", Von Nostrand Reinhold, New York, 5th Edition, 1998.*
2. *Gregg K. Hobbs, " Accelerated Reliability Engineering - HALT and HASS ", John Wiley & Sons, New York, 2000.*
3. *Lewis, " Introduction to Reliability Engineering ", 2nd Edition, Wiley International, 1996.*
4. *O' Connor, P.D.T., " Practical Reliability Engineering ", Hayden Book Company, New Jersey, 1981.*

AX038 VLSI Signal Processing	3	0	0	100

1. **9**

Introduction to DSP systems - Iteration Bound - Pipelined and parallel processing.

2. **9**

Retiming - Unfolding - Algorithmic strength reduction in filters and transforms.

3. **9**

Systolic architecture design - fast convolution - Pipelined and parallel recursive and adaptive filters.

4. **9**

Scaling and round off noise - Digital lattice filter structures - Bit level arithmetic architecture - Redundant arithmetic.

5. **9**

Numerical strength reduction - Synchronous, wave and asynchronous pipe lines - low power design - programmable digital signal processors.

Total No of periods: 45

AX038 VLSI Signal Processing **3 0 0 100**

Text Book:

1. Keshab K.Parthi, " VLSI Digital Signal Processing systems, Design and implementation ", Wiley, Inter Science, 1999.

References:

1. Mohammed Isamail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw-Hill, 1994.
2. S.Y. Kung, H.J. White House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
3. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

CM038	**Electromagnetic Interference and Compatibility in System Design**	**3**	**0**	**0**	**100**

1. EMI ENVIRONMENT **6**

Sources of EMI, counducted and radiated EMI, Transient EMI, EMI-EMC Definitions and units of parameters.

2. EMI COUPLING PRINCIPLES **9**

Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply Coupling.

3. EMI SPECIFICATION / STANDARDS / LIMITS **7**

Units of specifications, Civilian standards Military standards.

4. EMI MEASUREMENTS **7**

EMI Test Instruments /Systems, EMI Test, EMI Shielded Chamber, Open Area Test Site, TEM Cell Antennas, Conductors Sensors/Injectors/Couplers, Military Test Method and Procedures, Calibration Procedures.

5. EMI CONTROL TECHNIQUES **7**

Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

6. EMC DESIGN OF PCBS **9**

PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

Total No of periods: 45

CM038	**Electromagnetic Interference and Compatibility in System Design**	**3**	**0**	**0**	**100**

References:

1. Bernhard Keiser, " Principles of Electromagnetic Compatibility ", Artech house, 3rd Ed, 1986.
2. Henry W.Ott, " Noise Reduction Techniques in Electronic Systems ", John Wiley and Sons, 1988.
3. V.P.Kodali, " Engineering EMC Principles, Measurements and Technologies ", IEEE Press, 1996.

VL031 CMOS VLSI Design **3 0 0 100**

1. INTRODUCTION TO CMOS CIRCUITS **9**

MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, MOS Transistor Theory - Introduction MOS Device Design Equations, The Complementary CMOS Inverter-DC Characteristics, Static Load MOS Inverters, The Differential Inverter, The Transmission Gate, The Tri State Inverter, Bipolar Devices.

2. CIRCUIT CHARACTERSATION AND PERFORMANCE ESTIMATION **9**

Introduction, Resistance Estimation Capacitance Estimation, Inductance, Switching Characteristics CMOS-Gate Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing, Design Margining, Reliability.

3. CMOS CIRCUIT AND LOGIC DESIGN **9**

CMOS Logic Gate Design, Basic Physical Design of Simple Gate, CMOS Logic Structures, Clocking Strategies, I/O Structures, Low Power Design.

4. SYSTEMS DESIGN AND DESIGN METHOD **9**

Design Strategies CMOS Chip Design Options, Design Methods, Design Capture Tools, Design Verification Tools, Design Economics, Data Sheets, CMOS Testing - Manufacturing Test Principles, Design Strategies for Test, Chip Level Test Techniques, System Level Test Techniques, Layout Design for Improved Testability.

5. CMOS SUB SYSTEM DESIGN **9**

Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Zero/One Detectors, Binary Counters, ALUs, Multiplication, Shifters, Memory Elements, Control-FSM, Control Logic Implementation.

Total No of periods: 45

VL031 CMOS VLSI Design **3 0 0 100**

References:

1. *Nell H. E. Weste and Kamran Eshraghian, " Principles of CMOS VLSI Design ", 2nd Edition, Addision Wesley, 1998.*
2. *Jacob Backer, Harry W. Li and David E. Boyce, " CMOS Circuit Design, Layout and Simulation ", Prentice Hall of India, 1998.*

VL032	**Testing of VLSI Circuits**	**3**	**0**	**0**	**100**

1. **9**

Introduction - VLSI Testing Process And Test Equipment - Test Economics And Product Quality - Fault Molding-Logic And Fault Simulation.

2. **9**

Testability Measures - Combinational Circuit Test Generation-Sequential Circuit Test Generation.

3. **9**

Memory Test-Analog And Mixed Signal Test - Delay Test - IDDQ Test.

4. **9**

DFT Fundamentals - ATPQ Fundamental - Scan Architecture And Technique.

5. **9**

System Test-Embedded Core Test - Future Testing.

Total No of periods: **45**

VL032	**Testing of VLSI Circuits**	**3**	**0**	**0**	**100**

Text Books:

1. *Viswani D.Agarval Michael L.Bushnell, " Essentials of Electronic Testing for Digital Memory & Mixed Signal VLSI Circuit ", Kluwer Academic Publications, 1999.*
2. *Alfred L.Crouch " Design For Test For Digital IC's And Embedded Core Systems ", - PHI 1999.*

VL033	**Analog VLSI Design**	**3**	**0**	**0**	**100**

1. BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING **9**

Mixed-Singal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

2. BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING **9**

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensistive Silicon Retina.

3. SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS **9**

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Swtiched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators -Cascaded Architecture-Decimation Filters-mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

4. DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS **9**

Fault modeling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses-Design for Electron -Beam Testablity-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping analog Circuits.

5. STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT **9**

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

Total No of periods: 45

VL033 Analog VLSI Design **3 0 0 100**

Text Books:

1. *Mohammed Ismail, Terri Fiez, " Analog VLSI signal and Information Processing ", McGraw-Hill International Editons, 1994.*

References:

1. *Malcom R.Haskard, Lan C.May, " Analog VLSI Design - NMOS and CMOS "., Prentice Hall, 1998.*
2. *Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990.*
3. *Jose E.France, Yannis Tsividis, " Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994.*

VL034	**Low Power VLSI Design**	**3**	**0**	**0**	**100**

1. **9**

Introduction - Simulation - Power Analysis-Probabilistic Power Analysis.

2. **9**

Circuit -Logic - Special Techniques - Architecture and Systems.

3. **9**

Advanced Techniques - Low Power CMOS VLSI Design - Physics of Power Dissipation in CMOS FET Devices.

4. **9**

Power Estimation - Synthesis for Low Power - Design and Test of Low Voltages - CMOS Circuits.

5. **9**

Low Power Static RAM Architectures -Low Energy Computing Using Energy Recovery Techniques - Software Design for Low Power.

Total No of periods: 45

VL034 Low Power VLSI Design **3 0 0 100**

Text Books:

1. Gary Yeap " Practical Low Power Digital VLSI Design ", 1997.
2. Kaushik Roy, Sharat Prasad, " Low Power CMOS VLSI Circuit Design ", 2000.

VL035	**Design of Semiconductor Memories**	**3**	**0**	**0**	**100**

1. RANDOM ACCESS MEMORY TECHNOLOGIES **9**

Static Random Access Memories (SRAMs):
SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.
Dynamic Random Access Memories (DRAMs):
DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

2. NONVOLATILE MEMORIES **9**

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) Eproms-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

3. MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE **9**

RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

4. SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS **9**

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification.
Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures.

5. ADVANCED MEMORY TECHNOLOGIES AND HIGH-DENSITY MEMORY PACKAGING TECHNOLOGIES **9**

Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magnetoresistive Random Access Memories (MRAMs)-Experimental Memory Devices.
Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

Total No of periods: 45

VL035 Design of Semiconductor Memories **3 0 0 100**

Text Books:

1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ", Prentice-Hall of India Private Limited, New Delhi, 1997.