IK GUJRAL PUNJAB TECHNICAL UNIVERSITY

Scheme and Syllabus

of

Master of Technology

(VLSI Design)

Batch 2016

Semester-I								
Course Code	Course Title	L	T	P	Marks Distribution		Total Marks	Credits
					Internal	External		
MTRM-101	Research Methodology	3	1	0	50	100	150	4
MTVL-102	VLSI Design Concepts	3	1	0	50	100	150	4
MTVL-103	Hardware Description Languages	3	1	0	50	100	150	4
MTVL-104	VLSI Technology	3	1	0	50	100	150	4
MTVL-105	Design of Analog/ Mixed Mode VLSI Circuits	3	1	0	50	100	150	4
MTVL-106	Lab – I	0	0	4	100		100	2
	Total	**15**	**5**	**4**	**350**	**500**	**850**	**22**

Semester-II								
Course Code	Course Title	L	T	P	Marks Distribution		Total Marks	Credits
					Internal	External		
MTVL-201	Algorithms for VLSI Design Automation	3	1	0	50	100	150	4
MTVL-202	Testing and Fault Tolerance	3	1	0	50	100	150	4
MTVL-203	Embedded Systems	3	1	0	50	100	150	4
MTVL-	Elective-I	3	1	0	50	100	150	4
MTVL-	Elective-II	3	1	0	50	100	150	4
MTVL-204	Lab – II	0	0	4	100		100	2
	Total	**15**	**5**	**4**	**350**	**500**	**850**	**22**

Semester-III								
Course Code	Course Title	L	T	P	Marks Distribution		Total Marks	Credits
					Internal	External		
MTVL-	Elective-III	3	1	0	50	100	150	4
MTVL-	Elective-IV	3	1	0	50	100	150	4
MTVL-301	Project	0	0	4	100	50	150	4
MTVL-302	Seminar	0	0	2	50	-	50	1
MTVL-303	Dissertation(Synopsis)	0	0	6	-	-	-	S/US
	Total	**6**	**2**	**12**	**250**	**250**	**500**	**13**

Semester-IV								
Course Code	Course Title	L	T	P	Marks Distribution		Total Marks	Credits
					Internal	External		
MTVL-303	Dissertation	0	0	20	-	-	-	S/US
	Total	**0**	**0**	**20**	**-**	**-**	**-**	**-**

S-Satisfactory, US-Unsatisfactory

Elective-I

MTVL-205	Advanced Digital Signal Processing
MTVL-206	Semiconductor Devices
MTVL-207	VLSI Interconnects

Elective-II

MTVL-208	Memory Design and Testing
MTVL-209	Low Power VLSI Design
MTVL-210	Modeling and Simulation

Elective-III

MTVL-304	System on Chip (SOC)
MTVL-305	RF Circuit Design
MTVL-306	Advanced Computer Architecture
MTVL-307	Process and Device Characterization & Measurements

Elective-IV

MTVL-308	Sensor Technology and MEMS
MTVL-309	Nanoelectronics Devices
MTVL-310	Biomedical Electronics
MTVL-311	Hardware-Software Co-design

MTRM-101 Research Methodology

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Methods of Research: Nature and Objectives of research; historical, descriptive and experimental. Study and formulation of research problem. Scope of research and formulation of hypotheses; Feasibility, preparation and presentation of research proposal.

Introduction to Statistical Analysis: Measures of central tendency and dispersion: mean, median, mode, range, mean deviation and standard deviation. Regression and correlation analysis. Probability and probability distributions; Binomial, Poisson, Geometric, Negative binomial, Uniform, Exponential, Normal and Log-normal distribution. Basic ideas of testing of hypotheses; Tests of significance based on normal, t and Chi-square distributions. Analysis of variance technique.

Design of Experiments: Basic principles, study of completely randomized and randomized block designs. Edition and tabulation of results, presentation of results using figures, tables and text, quoting of references and preparing bibliography. Use of common softwares like SPSS, Mini Tab and/or Mat Lab. For statistical analysis.

Text Books / References

1. Borth Wayne C., The Craft of Research, Chicago Guides to Writing Edition and Publishing.
2. Johnson R.A., Probability and Statistics, PHI, New Delhi.
3. Meyer P.L., Introduction to Probability and Statistical, Applications, Oxford, IBH.
4. Hogg, R.V. and Craig A.T., Introduction to Mathematical Statistics, MacMillan.
5. Goon, A.M., Gupta, M.K. and Dasgupta, Fundamentals of Statistics, Vol. I: World Press.
6. Gupta, S.C. and Kapoor V.K., Fundamentals of Mathematical Statistics, Sultan Chand and Sons.

MTVL-102 VLSI Design concepts

Internal Marks:50	**L**	**T**	**P**
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Introduction To MOS Circuits: MOS Transistor Theory - Introduction MOS Device Design Equations, MOS Transistor as a Switches, Pass Transistor, CMOS Transmission Gate, Complementary CMOS Inverter, Static Load MOS Inverters, Inverters with NMOS loads, Differential Inverter, Tri State Inverter, BiCMOS Inverter, .

Circuit Characterization And Performance Estimation: Delay Estimation, Logical Effort and Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing, Design Margin and Reliability.

CMOS Circuit And Logic Design: CMOS Logic Gate Design, Physical Design of CMOS Gate, Designing with Transmission Gates, CMOS Logic Structures, Clocking Strategies, I/O Structures.

CMOS Sub System Design: Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Zero/One Detectors, Binary Counters, ALUs, Multipliers, Shifters, Memory Elements, Control- FSM, Control Logic Implementation.

Low Power CMOS VLSI Design: Introduction to Low Power Design, Power Dissipation in FET Devices, Power Dissipation in CMOS, Low-Power Design through Voltage Scaling – VTCMOS Circuits, MTCMOS Circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches, Low Power Basics CMOS Gate and Adder Design.

Texts / References

1. Sung Ms Kang, Yusuf Lablebici, “CMOS Digital Integrated Circuits: Analysis & Design”, Tata Mc-Graw Hill, 2011.
2. N. Weste and K. Eshranghian, "Principles of CMOS VLSI Design", Addison Wesley, 1998.
3. Neil H.E. Weste, David Harris, Ayan Banerjee,”CMOS VLSI Design:A Circuits and Systems Perspective ”, 2008.
4. Kiat-Seng Yeo, Kaushik Roy, “Low-Voltage, Low-Power VLSI Subsystems” – McGraw-Hil Professional ,2004.
5. Gary K. Yeap,”Practical Low Power Digital VLSI Design”, Kluwer Academic Press, 2002.
6. Jan M. Rabaey,”Digital Integrated Circuits: A Design Perspective”,Pearson Education.
7. Jacob Backer, Harry W. Li and David E. Boyce, " CMOS Circuit Design, Layout and Simulation ", Prentice Hall of India.

MTVL-103 Hardware Description Languages

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Basic concepts of Hardware Description Languages: VLSI Design flow**,** Features of VHDL, Capabilities, Hierarchy, Syntax and Semantics of VHDL; Basic Language Elements- Data objects- Variable signal, and constant, Data types, Operators and signal assignments, Design Suits- Entities, architecture declaration, configurations, Packages.

Modeling Styles (VHDL): Behavioral Modeling- Process statement, Sequential assignment statements, Loops, wait statement, assertion statement, Delay Model – Inertial delay Model, Transport delay model; Gate Level Modeling – Component instantiation statements; Data flow Modeling - Concurrent assignment statement, Conditional assignment statements, Procedures, functions, Generics, attributes, Model simulation- Writing a test bench, Logic Synthesis.

Introduction to Verilog Hardware Description Language: Key features, Capabilities, Language Constructs and Conventions in Verilog, Syntax and Semantics of Verilog; Basic Language Elements: Operators, nets, registers, vectors, arrays, parameters, system tasks, complier directives, Module, port connection rules,

Modeling Styles (Verilog): Gate Level Modeling- Gate types, Gate delays; Dataflow Modeling – continuous assignment, Behavioral Modeling- Initial & Always Construct, Assignments with Delays, wait construct, Multiple always blocks, If and if-else, assign, Loop Construct, Sequential and Parallel blocks, Switch level modeling- MOS switches, CMOS switches.

Design using VHDL/Verilog Unit- Combinational logics- Adder, Subtractor, Decoders, Encoders, Multiplexer, code Converter; Flip flop, state machines – Mealy type FSM, Moore type FSM, Counters and Shift register. Synthesis of digital logic circuits.

Text / References

1. J. Bhaskar, "A VHDL Primer, 3rd Edition, Pearson Education
2. Douglas Perry, "VHDL", McGraw Hill International, New York, 1993.
3. S. Brown & Z. Vransesic, “Fundamental of digital Logic with Verilog design”, Tata McGraw Hill.
4. S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall (NJ, USA), 1996.
5. Frank Vahid, “Digital Design”, Wiley, 2006
6. Peter J Ashenden, “The Designer’s Guide to VHDL”, Morgan Kaufmann Publishers.
7. Navabi, “VHDL Analysis & Modeling of digital systems”, McGraw Hill, 1998.

MTVL-104 VLSI Technology

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.

Impurity incorporation: Solid State diffusion modeling and technology; Ion Implantation modeling, technology and damage annealing; characterization of Impurity profiles.

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation Technologies in VLSI and ULSI; Characterization of oxide films; High k and low k dielectrics for ULSI.

Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI;Mask generation.

Chemical Vapour Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modeling and technology.

Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal Interconnects; Multi-level metallization schemes.

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI.

Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology

Text/References

1. S.M.Sze (Ed), "VLSI Technology", 2nd Edition, McGraw-Hill, 1988.Streetman," VLSI Technology".
2. C.Y. Chang and S.M. Sze (Ed), "ULSI Technology", McGraw-Hill Companies Inc., 1996.
3. S.K.Gandhi, "VLSI fabrication Principles",John Wiley Inc., New York, 1983.
4. VLSI Fabrication Technology ,B.Raj & Singh , Laxmi Publications

5. Sorab K. Gandhi, "The Theory and Practice of Microelectronics", JohnWiley & Sons
6. B.G Streetman, "VLSI Technology" , Prentice Hall, 1990.
7. A.S Grove, "Physics and Technology of semiconductor devices", John Wiley & Sons

MTVL-105 Design of Analog/ Mixed Mode VLSI Circuits

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

- Basic CMOS Circuit Techniques, Continuous Time And Low voltage Signal Processing: Mixed-Signal VLSI Chips, Analog MOSFET Modelling: MOS transistor, Low frequency MOSFET Models, High frequency MOSFET Models, Temperature effects in MOSFET, Noise in MOSFET.
- Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor- Primitive Analog Cells, Current Source, Sinks and References MOS Diode/Active resistor, Simple current sinks and mirror, Basic current mirrors, Advance current mirror, Current and Voltage references, Bandgap references.
- CMOS Amplifier Performances matrices of amplifier circuits, Common source amplifier, Common gate amplifier, Cascode amplifier, Frequency response of amplifiers and stability of amplifier.
- CMOS Differential Amplifier Differential signalling, source coupled pair, Current source load, Common mode rejection ratio, CMOS Differential amplifier with current mirror load,, Differential to single ended conversion. Linear Voltage-Current Converters- CMOS, Bipolar and Low- Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design.
- Basic BiCMOS Circuit Techniques, Current -Mode Signal Processing: Continuous-Time Signal Processing- Sampled-Data Signal Processing-Switched-Current Data Converters.
- Sampled-Data Analog Filters, Over Sampled A/D Converters and Analog Integrated Sensors: First-order and Second SC Circuits-Bilinear Transformation – Cascade Design-Switched-Capacitor Ladder Filter
- Analog VLSI Interconnects: Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping analog Circuits.

Text/References

1. Design of Analog CMOS Integrated Circuits by Behzad Razavi McGraw Hill.
2. Mohammed Ismail, Terri Fiez, " Analog VLSI signal and Information Processing ", 1994, McGraw-Hill International Editons.
3. CMOS: Circuit Design , Layout and Simulation by R. Jacob Baker, Harry W. Li, and David E. Boyce, Prentice Hall of India
4. Analog Integrated circuit Design by David A. Johns and Ken Martin, John Wiley & Son
5. Greogorian & Tames, " Analog Integrated Circuit For Switched Capacitor Circuit "

MTVL-106 Lab – I

Internal Marks:100	**L**	**T**	**P**
External Marks: -	**0**	**0**	**4**
Total Marks:100			

2 Bit-Counter: The purpose of this lab is to write a HDL description of 2-bit counter as a finite state machine. The 2-bit counter has several inputs such as clk, rst, enable, load, count-up or count-down etc.

Parallel to Serial Converter: The purpose of this lab is to write a HDL description of a parallel to serial converter as an FSMD. The parallel to serial converter will accept an eight-bit number and send one bit of data over the data line per clock cycle. There is also a go bit, which tells the converter to start transmitting data.

VHDL Calculator: The purpose of this lab is to implement a finite state machine in VHDL to perform simple calculations like addition, subtraction, and multiplication

A Simplified HDL UART: In this lab the students design a UART to send data to the PC.

I^2C Bus: HDL implementation of I2C bus protocol

Design of a Hardware Multiplier: In this lab students are going to implement hardware multiplier using Sequential Circuit Components.

ALU Design: The purpose of this lab is to build a 4/8 -bit ALU. The ALU is written behaviorally. It should take in two numbers and be able to add the numbers, subtract the numbers, NOR the numbers, or NAND the numbers.

NMOS Inverter: Depletion and enhancement mode inverter circuit simulation and modification in circuit parameters.

CMOS Inverter: Circuit simulation, adjustment of W / L ratio of P & N channel MOS transistor for symmetrical drive output and loading consideration. Scaling of CMOS Inverter for different technologies,study of secondary effects (temperature, power supply and process corners). Layout of CMOS Inverter, extraction of parasitics and back annotation and related modifications in circuit parameters and layout.

Current Source / Mirror: Circuit simulation of current mirror using BJT and MOS (Simple, Wilson and Widler configurations) study and modifications to improve power and load regulation. Layout of CMOS current mirror.

8 Bit shift register cell: Building of cell Library of logic gates and flip flops and building of 8 bit shift register from the same. Optimization of the same from layout and power considerations.

Differential Amplifier: Study of specifications of differential amplifier and design considerations. Study of input loading and biasing techniques.

MTVL-201 Algorithms for VLSI Design Automation

Internal Marks:50	**L**	**T**	**P**
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Logic synthesis & verification: Introduction to combinational logic synthesis, Binary decision diagram, Hardware models for High-level synthesis.

VLSI automation Algorithms Partitioning: Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

Placement, floor planning & pin assignment: Problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

Detailed routing: Problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

Texts / References

1. Naveed Shervani, "Algorithms for VLSI physical design Automation" Kluwer Academic Publisher, 3rd edition, 1999.
2. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
3. Rolf Drechsheler : "Evolutionary Algorithm for VLSI CAD" 2nd edition, Kluwer Academic publisher,2010.
4. Trimburger, "Introduction to CAD for VLSI" Kluwer Academic publisher, 2002.

MTVL-202 Testing and Fault Tolerance

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Introduction to Testing: Role of testing VLSI circuits, VLSI trends affecting testing, Physical Faults, Stuck-at Faults, Stuck open Faults, Permanent, Intermittent and Pattern Sensitive Faults, Delay Faults.

Fault Modeling- Functional Testing, Structural Testing, Types of Fault Models, Stuck-at Faults, Bridging Faults, cross point faults, Fault Equivalence, Fault Dominance

Fault Simulation- Design Verification, Modeling Levels and Types of Simulators, True value simulation algorithm - Compiled-Code, Event-Driven; Fault Simulation algorithm- Serial, Parallel, Deductive and Concurrent Fault Simulation.

Testability Measure – Controllability, Observability, SCOAP measures for combinational and sequential circuits.

ATPG for Combinational Circuits: Path Sensitization Methods, Roth's D- Algorithm, PODEM Algorithm, Complexity of Sequential ATPG, Time Frame Expansion.

Design for Testability- Ad-hoc, Structured DFT- Scan method, Scan Design Rules, Overheads of Scan Design, Built In Self Test- System level Diagnosis, LFSR, Exhaustive, pseudorandom test pattern Generation, BILBO, Pseudo-Random Pattern Generation, Weighted Pseudo-Random Pattern Generation, response compaction - Parity checking, Ones counting, Transition Count, Boundary Scan Standard - TAP Controller, Test Instructions.

Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction codes, Reconfiguration Techniques, Yield Modelling Reliability.

Text Books/ References

1. Michael L.Bushnell, Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital Memory & Mixed Signal VLSI Circuits", Kluwer Academic Publications, 1999.
2. Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman, " Digital Systems Testing and Testable Design", 3rd Edition, Jaico Publishing House, 2004
3. Hideo Fujiwara, " Logical testing & design for testability", The MIT Press.
4. Mike Tien Chienlee, "High level Test Synthesis of Digital VLSI circuits", Artech ouse Boston London.

MTVL-203 Embedded Systems

Internal Marks:50	**L**	**T**	**P**
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

- Introduction And Examples Of Embedded Systems, Concept Of Embedded System Design: Design challenge, Processor technology, IC technology, Design technology, Trade-offs. Custom single purpose processor hardware, general-purpose processor: introduction, basic architecture, operation, super-scalar and VLSIIW architecture, application specific instruction set processors (ASIPS), microcontrollers, digital signal processors, selecting a microprocessor.

- Memory: Introduction, Memory write ability, Storage performance, Tradeoff s, Common memory types Memory hierarchy and cache AVR 8515 microcontroller: Architecture and Programming in assembly and C. Interfacing Analog and digital blocks: Analog-to-Digital Converters (ADCs), Digital to Analog, Converters (DACs)., Communication basics and basic protocol concepts, Microprocessor interfacing: I/O addressing, Port and Bus based, I/O, Memory mapped I/O, Standard I/O interrupts, Direct memory access, Advanced communication principles parallel, serial and wireless, Serial protocols I2C, Parallel protocols PCI bus, Wireless protocol IrDA, blue tooth.· Different peripheral devices: Buffers and latches, Crystal, Reset circuit, Chip select logic circuit, timers and counters and watch dog timers, Universal asynchronous receiver, transmitter (UART), Pulse width modulators, LCD controllers, Keypad controllers.

- Design tradeoffs due to thermal considerations and Effects of EMI/ES etc.Software aspect of embedded systems: Challenges and issues in embedded software development, Co-design

- Embedded software development environments: Real time operating systems,Kernel architecture: Hardware, Task/process control subsystem, Device drivers, Filesubsystem, system calls, Embedded operating systems, Task scheduling in embedded systems: task scheduler, first in first out, shortest job first, round robin, priority based scheduling, Context switch: Task synchronization: mutex, semaphore, Timers.

- Types of embedded operating systems, Programming languages: assembly languages, high level languages for embedded systems: Embedded system development process Determine the requirements, Design the system architecture, Choose the operating system, Choose the processor, Choose the development platform, Choose programming language, Coding issues, Code optimization, Efficient input/output Testing and debugging, Verify the software on the host system, Verify the software on the embedded system.

BOOKS / REFERENCES

1. Frankvahid/Tony Givargis, " Embedded System Design- A unified Hardware/software Introduction".
2. David E Simon, " An embedded software primer ", Pearson education Asia, 2001.
3. Dreamteach Software team," Programming for Embedded Systems" AVR 8515 manual
4. J.W. Valvano, "Embedded Microcomputor System: Real Time Interfacing"
5. Jack Ganssle, "The Art of Designing Embedded Systems", Newnes, 1999.

MTVL-205 Advanced Digital Signal Processing

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

- Transformations: Review of Fourier Transforms, Z-Transforms, Discrete Fourier Transform, Fast Fourier Transform, Convolution and Correlation.
- Design of digital filters: introduction to filter design, types of digital filters, choosing between, fir and iir filters, filter design steps, effect of finite register length in filter design, realization of iir digital filters and fir digital filter, design of iir filters from continuous time filters, design of fir filters by windowing.
- Spectrum estimation: non-parametric methods correlation method, co-variance estimator, performance analysis of estimators, consistent estimators, ar, ma, ARMA signal modeling parameter estimation using Yule-walker method.
- Linear estimation and predication: maximum likelihood criterion efficiency of estimator, least mean squared error criterion, recursive estimators, and linear predications.
- Multirate digital signal processing: Mathematical description of change of sampling rate, interpolation and decimation, continuous time model, direct digital domain approach, interpolation and decimation by an integer factor, single and multistage realization, applications of sub band coding.
- Adaptive Filters: Applications Of Adaptive Filters, Adaptive Direct Form FIR Filters: The LMS Algorithm, Adaptive Lattice Ladder Filters, Recursive Least Squares Lattice Ladder Algorithms.
- DSP Chips: Introduction to fixed point and floating point processors, ADSP21xx and TMS320Cxx-Architecture, Memory, Addressing Modes, Interrupts, Applications. Comparison of ADSP21xx and TMS320Cxx series.

BOOKS / REFERENCES

1. Emmanuel C.Ifeachor Barrie W.Jervis, “Digital Signal Processing”, Pearson Education Asia
2. Proakis, Manolakis ,” Digital Signal Processing principles, algorithms, andapplications”, Prentice Hall India
3. “Digital Signal Processing”, by S.K.Mitra, -Tata-Mcgraw Hill.
4. ADSP 2181 manuals
5. Keshab K. Parhi, ” VLSI DSP Systems; Design & implementation” , WileyInterScience Publishers
6. John G. Proakis, Charles M. Rader, Fuyun Ling, Chrysostomos L. Nikias, Marc Moonen, Ian k. Proudler, ”
7. Algorithms for statistical signal processing”, Pearson Education Asia.

MTVL-206 Semiconductor Devices

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Semiconductor Physics Fundamentals: Quantum Mechanics Concepts, Schrodinger wave equation, Carrier Concentration, Drift Velocity, Diffusion Transport Equation, Mobility effects, Hall Effect, Continuity Equation, Carrier Generation and Recombination, Shockley Read Hall Theory of Recombination.

PN Junction: Energy band diagrams, Step junction, linearly graded junction, I-V Characteristics, Junction break down Phenomenon- Zener, Avalanche Process.

Bipolar Junction Transistor: Introduction to BJT, Transistor Action, Minority carrier distribution profile, Equivalent Models -Ebers - Molls Model, Gummel Poon Model, Non-ideal effects in BJT- Early effect, High Injection etc.

MOSFET Modeling: Introduction Interior Layer, MOS Transistor Current, Energy band diagram, Threshold Voltage, Work function difference, Flat band voltage, Depletion layer thickness, Charge distribution, C-V characteristics, I-V Characteristics.

Non-ideal Effects in MOSFET: Short Channel and Narrow Width Effect, Sub-threshold Conduction, Channel length modulation, Velocity saturation, , V_T roll-off, Dain Induced Barrier Lowering, Gate Induced Drain Leakage, Gate Tunneling, Punch through.

Emerging Nano- Devices – Introduction to Nano-devices and structures, Transport Phenomenon.

Text Books / References

1. Donald A. Neamen, “Semiconductor Physics and Devices, 3rd Edition, McGraw Hill, 2007.
2. Ben G. Streetman, Sanjay Banerjee, “ Solid state electronic devices”, Pearson Education, 7th Edition, 2014.
3. Edward S. Yang, “Fundamentals of Semiconductor Devices”, Mc-Graw Hill.
4. S.M. Sze, "Physics of Semiconductor Devices", Wiley Eastern, 1981.
5. Tsividis, Yannis, “Operation and modeling of the MOS transistor”, Oxford University Press, 2nd Edition, 1999
6. Sedra, Smith, “Microelectronic Circuits”
7. E.H. Nicollian and J.K. Brews, "MOS physics and technology", John Wiley, 1982.
8. Richard S. Muller and Theodore I. Kamins “Device Electronics for Integrated Circuits”, John Wiley and Sons.
9. Pail Richman, “MOS Field Effect Transistor and Integrated Circuits”, John Wiley and Sons.

MTVL-207 VLSI Interconnects

Internal Marks:50	**L**	**T**	**P**
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Interconnects

Interconnect Parameters: Resistance, Inductance, and Capacitance, Interconnect RC Delays:Elmore Delay Calculation. Interconnect Models: The lumped RC Model, the distributed RC Model, the transmission line model. SPICE Wire Models: Distributed RC lines in SPICE, Transmission line models in SPICE.

Scaling issues in interconnects

Gate and Interconnect Delay

CMOS Repeater

The Static Behavior- Switching Threshold, Noise Margins, The Dynamic Behavior- Computing the capacitances, Propagation Delay: First order Analysis, Propagation Delay from a Design perspective, Power, energy and Energy-Delay- Dynamic Power Consumption, Static Consumption, Analyzing Power Consumption using SPICE

Repeater Design: Driving Interconnects for Optimum speed and power

Short channel model of CMOS Repeater - Transient Analysis of an RC loaded CMOS repeater, Delay Analysis, Analytical power expressions: Dynamic power, Short circuit Power, Resistive Power Dissipation, CMOS Repeater insertion: Analytical expressions for delay and power of a repeater chain driving an RC load.

Advanced Interconnect Techniques

Reduced-swing Circuits, Current-mode Transmission Techniques

Crosstalk

Theoretical basis and circuit level modeling of crosstalk, Energy dissipation due to crosstalk: Model for energy calculation of two coupled lines. Contribution of driver and interconnect to dissipated energy, Crosstalk effects in logic VLSI circuits: Static circuits, Dynamic circuits and various remedies.

Texts / References

1. John P. Uymera, Introduction to VLSI Circuits and Systems, Wiley Student Edition.
2. S.M. Kang, L. Yusuf, CMOS Digital Integrated Circuits-Analysis and Design TMH, 3rd Edition.
3. Jan M. Rabaey, Analysis and Design of Digital Integrated Circuits– A design Perspective, TMH, 2nd Edition 2003.
4. F.Moll, M.Roca, Interconnection Noise in VLSI Circuits, Kluwer Academic Publishers.

MTVL-208 Memory Design and Testing

Internal Marks:50	**L**	**T**	**P**
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Random Access Memory Technologies: Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.

Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures -BiCMOS DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

Nonvolatile Memories: Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) -Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMS-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

Memory Fault Modeling: Testing, And Memory Design For Testability And Fault Tolerance RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing. Semiconductor Memory Reliability and Radiation Effects.

Texts / References

1. A.K Sharma, “Semiconductor Memories Technology, Testing and Reliability”, illustrated Edition, IEEE Press, 1997.
2. Gerald Luecke, Jack P. Mize, William N. Carr, “Semiconductor Memory design & application”, illustrated Edition,Mc-Graw Hill, 1973.
3. Memory Technology design and testing, IEEE International Workshop on: IEEE Computer Society Sponsor (S), 1999.
4. Parag K. Lala ,“An Introduction to Logic Circuit Testing” Morgan & Claypool Publishers, 2009.
5. Viswani D.Agarval Michael L.Bushnell, “Essentials of Electronic Testing for Digital Memory & Mixed Signal VLSI Circuit” Kluwer Academic Publications, 1999.

MTVL-209 Low Power VLSI Design

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Introduction: Need for low power VLSI chips, Sources of power dissipation in Digital Integrated circuits. Emerging low power approaches. Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Power Estimation: Simulation Power analysis- SPICE circuit simulators, Gate level logic simulation, Capacitive power estimation, Static state power, Gate level capacitance estimation, Architecture level analysis, Data correlation analysis in DSP systems. Monte Carlo simulation. Probabilistic power analysis- Random logic signals, Probability & frequency, Probabilistic power analysis techniques.

Low Power Design: Circuit level- Power consumption in circuits, Flip Flops & Latches design, High capacitance nodes, Low power digital cells library Logic level- Gate reorganization, Signal gating, Logic encoding, State machine encoding, Precomputation logic.

Low Power Architecture & Systems: Power & performance management, Switching activity reduction, Parallel architecture with voltage reduction, Flow graph transformation, Low power arithmetic components, Low power memory design.

Low Power Clock Distribution: Power dissipation in clock distribution, single driver vs distributed buffers, zero skew vs tolerable skew, chip & package co design of clock network.

Algorithm & Architectural Level Methodologies: Introduction, design flow, algorithmic level analysis & optimization, architectural level estimation & synthesis.

Texts / References

1. Kaushik Roy, Sharat Prasad, Low-Power CMOS VLSI Circuit Design, Wiley, 2000
2. Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP, 2002
3. Rabaey and Pedram, Low power design methodologies, Kluwer Academic,1997.
4. A. Bellamour, M. I. Elamasri, Low Power CMOS VLSI Circuit Design, Kluwer Academic Press, 1995.
5. Siva G. Narendran, Anatha Chandrakasan, Leakage in Nanometer CMOS Technologies, Springer, 2005.
6. Sung-Mo Kang, Yusuf Leblebici CMOS Digital Integrated Circuits – Analysis and Design , TMH, 2011.

MTVL-210 Modelling and Simulation

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Component model for ICs: Design rule checks, timing verification worst case delay simulation, setup and hold times for clocked devices; Behaviour modeling, structural modeling, simulation with the physical model; Hardware Description Language.

Statistical: Description of data, Data-fitting methods, Regression analysis, Analysis of Variance, Goodness of fit.

Probability and Random Processes: Discrete and Continuous Distribution, Central Limit theorem, Measure of Randomness, Monte Carlo Methods.

Stochastic Processes: Stochastic Processes and Markov Chains, Time Series Models.

Modelling and simulation: Concepts, Discrete-event simulation: Event scheduling/Time advance algorithms, Verification and validation of simulation models.

Continuous simulation: Modelling with differential equations, Example models, Bond Graph Modelling, Population Dynamics Modelling, System dynamics.

Texts / References

1. James R., Armstrong J.R., Chip-level Modelling with VHDL., Prentice Hall, 1989.
2. Navalih, Z., VHDL, Analysis and Modelling of Digital Systems, 1993.
3. Banks J, Carson JS and Nelson B, discrete-Event System simulation, 2nd Edition, Prentice-Hall of India, 1996.
4. Winston, W.L., Operations Research : applications and algorithms, 3rd Edition, Duxbury press, Belmont, Califomia, 1994.

MTVL-204 Lab – II

	L	T	P
Internal Marks:100			
External Marks: -	**0**	**0**	**4**
Total Marks:100			

Arithmetic Unit (8-bit): Designing the Specifications and circuit of an Arithmetic Unit. Implementation of an Arithmetic Unit on FPGA.

Multiplexed Display Controller: Designing the Specifications and circuit of a Multiplexed Display Controller (MDC) Implementation of a Multiplexed Display Controller on FPGA.

Scanned Keyboard Controller: Designing the Specifications and circuit of a Scanned Keyboard Controller. Implementation of a Scanned Keyboard Controller on FPGA.

UART: Designing the Specifications and circuit of a UART. Implementation of a UART on FPGA.

CRT Controller: Designing the Specifications and circuit of a CRT Controller. Implementation of a CRT Controller on FPGA.

Filter Implementation using MAC: Designing the Specifications and circuit of a Filter Implementation using MAC. Implementation of a MAC on FPGA.

Decimal Counter and Multiplexing the Output: The purpose of this lab is to implement a decimal counter, which counts from 0 to 99. The students will be required to write a program for the AVR 8515 micro-controller.

Watchdog Timer: In this lab the students will design a hardware watchdog timer. They are ment to write a buggy program in order to test their WDT. The 8515 program should perform some computation, e.g., write 1, 2, 3 ... to the LED and at some point enter an infinite loop. During normal operation, the 8515 program must periodically (up to 254 second long cycles) write to the WDT's initial value register to avoid unnecessary resets.

AVR microcontroller UART in C: Implement AVR microcontroller UART in C

Implementation of simple calculator using AVR 8515: Implement a simple calculator using AVR 8515 microcontroller with keyboard and LCD display interface.

Analog to Digital Conversion: To implement analog to digital conversion using the ADC0804LCN 8-bit A/D converter. You will design a circuit and program the chip so that when an analog signal is given as input, the equivalent digital voltage is displayed on an LCD display.

Implementing SPI bus Using AVR 8515: To implement I2C serial communication using AVR 8515. Digital Filters with AVR Implement digital filters using low cost microcontroller from AVR series. Converting 8-bit LCD communication to 4-bit

IR Remote Control Receiver: In this lab students are required to design and implement IR remote control receiver using AVR 8515 microcontroller.

Step Motor Controller: In this lab students are meant to implement a compact size and high-speed interrupt driven step motor controller.

MTVL-304 System on Chip (SOC)

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

System on Chip Design: Technology Challenges in System on a Chip (SOC) components. SoC Design Methodology , Moving to System-on-Chip Design, Overview of the SOC Design Process, Canonical SoC Design, System Design Flow, System Architecture, Components of the system, Hardware & Software, Processor Architectures, System Architecture and Complexity. Parameterized Systems-on-a-Chip , System-on-a-chip Peripheral Cores .

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split Caches, Multilevel Caches, Virtual to real translation, SOC Memory System, Models of Simple Processor –memory interaction.

Designing Communications Networks: Basic Architectures, SOC Standard Buses. Interconnect Customization and Configuration: Interconnect latency modeling, Inter Connect Architectures, Introduction to AMBA bus. Concept of PLB-processor local bus and OPB-on chip peripheral bus. Network on Chip ,

Verification: System Level, Block Level and Hardware/Software Co-verification, SOC components: emulation, co-simulation, Physical Verification.

Application Studies / Case Studies: AES algorithmsImage compression, VOIP, antenna for SOC etc

Text/References

1. Wayone Wolf," Modern VLSI Design: SOC Design"
2. Prakash Rashnikar, Peter Paterson, Lenna Singh" System-On-A-Chip Verification methodology & Techniques", Kluwer Academic Publishers.
3. Alberto Sangiovanni Vincentelli," Surviving the SOC Revolution: A Guide to Platform- based Design", Kluwer Academic Publishers.
4. Design of System on a Chip: Devices and Components –Ricardo Reis, 1st Ed., 2004, Springer

MTVL-305 RF Circuit Design

Internal Marks:50	**L**	**T**	**P**
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

- Introduction to RF and Wireless Technology: Complexity, design and applications. Choice of Technology. Basic concepts in RF Design: Nonlinearly and Time Variance, intersymbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion.
- Analog and Digital Modulation for RF circuits: Comparison of various techniques for power efficiency. Coherent and Non coherent defection. Mobile RF Communication systems and basics of Multiple Access techniques.
- Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct Conversion and two steps transmitters. BJT and MOSFET behaviour at RF frequencies modelling of the transistors and SPICE models. Noise performance and limitation of devices. Integrated parasitic elements at high frequencies and their monolithic implementation.
- Basic blocks in RF systems and their VLSI implementation: Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range. Various Mixers, their working and implementations.
- Oscillators: Basic topologies VCO and definition of phase noise. Noise-Power trade-off. Resonator less VCO design. Quadrature and single-sideband generators, Radio Frequency Synthesizes: PLLS, Various RF synthesizer architectures and frequency dividers.
- Power Amplifiers design. Linearization techniques, Design issues in integrated RF filters, Some discussion on available CAD tools for RF VLSI designs.

Texts / References

1. B.Razavi, RF Microelectronics, Prentice-Hall PTR,1998.
2. T.H.Lee, The Design of CMOS Radio-Frequency Integrated Circuits", Press, 1998.
3. R.Jacob Baker,H.W.Li, and D.E. Boyce, CMOS Circuit Design ,Layout and Simulation, Prentice-Hall of ,1998.
4. Y.P. Tsividis Mixed Analog and Digital VLSI Devices and Technology, McGraw Hill,1996.

MTVL-306 Advanced Computer Architecture

Internal Marks:50	**L**	**T**	**P**
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputer, Multivector and SIMD computers.

Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms.

System Interconnect Architectures: Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.

Advanced processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors.

Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines.

Multiprocessor architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization.

Texts / References

1. Recommended Books 1. Kai Hwang, “Advanced computer architecture”18th reprint, TMH,2003.
2. D. A. Patterson and J. L. Hennessey, “Computer organization and design,” 4th edition, Morgan Kaufmann.
3. J.P.Hayes, “computer Architecture and organization” 2 nd Edtion; MGH, 1988.
4. Harvey G. Cragon, “Memory System and Pipelined processors” Narosa Publication, 1996.
5. V.Rajaranam & C.S.R.Murthy, “Parallel computer” PHI.
6. R.K.Ghose, Rajan Moona & Phalguni Gupta, “Foundation of Parallel Processing” Narosa Publications.

MTVL-307 Process and Device Characterization & Measurements

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Resistivity: Wafer mapping, two point versus four point probe, resistivity profiling (differential hall effect, spreading resistance profiling), contactless methods.

Carrier Doping: Capacitance-voltage(C-V), current-voltage(I-V), optical techniques. Contact resistance and Schottky Barriers: metal-semiconductor contacts, measurement techniques, schottky barrier height.

Defects: Generation-recombination statistics, deep-level transient Spectroscopy (DLTS), Carrier life time: recombination lifetime/surface recombination velocity, generation lifetime/surface generation velocity.

Recombination lifetime: Optical measurements : photoconductance decay, quasi-steady state photoconductance,free carrier absorption, electron beam induced current, short circuit current/open circuit voltage decay. Recombination lifetime-electrical measurements: diode current-voltage, reverse recovery, open circuit voltage decay, pulsed MOS capacitor. Generation lifetime-Electrical measurements: gate-controlled diode, pulsed MOS Capacitor.

Physical Characterization: Thin Film Thickness-Measurements-ellipsometry, surface profiling, spectrophotometry, FTIR Critical Dimension Measurements: Optical microscope, Scanning Electron Microscope, Transmission Electron Microscope Material and Impurity Characterization: SIMS, XRD, EDAX Electrical Characterization:, sheet resistance C-V measurements, DLTS, Carrier lifetime, impurity profiling, I-V measurements, Process and SPICE model parameter Extraction.

Texts / References

1. W.R. Reunyan, “Semiconductor Measurements and Instrumentation”, Mc-Graw Hill, 2nd Edition, 1998.
2. Schroder, “Semiconductor Material And Device Characterization”, 2nd edition, Wiley-Interscience, 2nd edition, 1998.
3. Philips F. Kare and Greydon B. Lauabee, “Characterization of semiconductor Materials”, Mc-Graw Hill, 2nd edition, 2000.
4. K.V. Ravi, “Imperfections and Impurities In Semiconductor Silicon”, John Wiley & Sons Inc., 1st edition, 1981.
5. Tor A. Fjeldly, Trond Ytterdal, Michael Shur “Introduction to device modeling and circuit simulation” Wiley, 3rd edition, 1998.
6. By Jianjun Gao “Optoelectronic Integrated Circuit Design and Device Modeling” Wiley, 2011.

MTVL-308 Sensor Technology and MEMS

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Introduction

Historical Development of Microelectronics, Evolution of Micro sensors, Evolution of MEMS, Emergence of Micro machines, Sensor Systems, Sensors types and classification, Mechanical Sensors, Acoustic Sensors, Magnetic Sensors, Thermal Sensors, Optical sensors Chemical Sensors, Radiation Sensors and Biosensors. Micro sensors, Sensors based on surface-acoustic wave devices. Review Of Fabrication Techniques (Lithography, PVD,CVD,RIE)

Micromachining techniques

Introduction to Bulk Micromachining, Isotropic and Orientation-Dependent Wet Etching, Dry Etching, Buried Oxide Process, Silicon Fusion Bonding, Sacrificial Layer Technology, Surface Micromachining using Plasma Etching, ,Combined 1C Technology and Anisotropic Wet Etching, Processes Using Both Bulk and Surface Micromachining, Adhesion Problems in Surface Micromachining, Surface Versus Bulk Micromachining

Smart Sensors and Modeling

Introduction to Smart Sensors, Integrated Smart sensors and smart systems, MEMS and NEMS devices, Elastic structures in MEMS and NEMS, Modeling of Thermal Elastic systems, Electrostatic- elastic systems, magnetically actuated systems, Microfluidics (Membrane Pumps, Nanolithography, Nano jets)

Texts / References

1. Modeling MEMS and NEMS John A. Pelesko and David H. Bernstein Chapman & Hall/CRC
2. MEMS Fundamental Technology and Applications vikas Choudhary and Krzysztof Iniewski CRC press
3. Micro sensors, MEMS and Smart devices Julian W. Gardner ,Vijay K. Varadan John Wiley & Sons, Ltd
4. Smart Sensor Systems Edited by Gerard C.M. Meijer © 2008 John Wiley & Sons, Ltd.
5. Ristic L (ed), “Sensor Technology and Devices”, Artech House, London, 1994.
6. Sze S.M. (ed), “Semiconductor Sensors”, John Wiley, New York, 1994 Wise
7. K.D. (Guest Editor) “Integrated Sensors, Microp-actuators and micro-systems
8. MEMS, Special Issue of proceedings of IEEE, Vol. 86, No.8, August 1998.

MTVL-309 Nanoelectronics Devices

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Introduction: Moore's Law and Its Significance, Size Dependent Electrical Properties in Nanomaterials: Matthiessen's Rule, Development of Nanoelectronics; Strategies for Fabrication of Nano Devices; Development of Electronics: Semiconductor Transistors; Some Tools of Micro and Nanofabrication.

Quantum Electronic Devices: High Electron Mobility Transistors; Quantum Interference Transistors; Single Electron Transistors; Quantum Corrals; Carbon Nanotube Transistors; Quantum Computers: Working of Quantum Computer, Difference Between Quantum and Classical Computer, Decoherence, Experimental Implementation of Quantum Computers.

Nanobiometrics: Lipids as Nano-Bricks and Mortar; Self-Assembled Monolayers; The Bits that Do Things-Proteins: 3D Optical Memory, Basic Concepts on Molecular Machines and Nanoscale Motors, Nanovalves; Structure is Information-DNA: Smart Glue, Wire Template; A Biological Nanotechnology Future.

Photonics and Solar Energy: Properties of Light and Nanotechnology, Interaction of Light and Nanotechnology: Photon Trapping and Plasmons, Dielectric Constant and Polarization; Nanoholes and Photons; Imaging; Energy Efficient Windows and Solar Absorbers Based on Nanoparticles.

Texts / References

1. Nanoscience; The Science of the Small in Physics, Engineering, Chemistry, Biology and Medicine by Hans-Eckhardt Schaefer (Springer).
2. Carbon Nanotubes: Science and applications by Laurie Kelly and Meyyappan (CRS Press).
3. Handbook of Nanofabrication by Gary P. Wiederrecht (Ed.) (Elsevier)
4. Molecular electronic devices by F.L. Carter et al (Ed).

MTVL-310 Biomedical Electronics

Internal Marks:50	**L**	**T**	**P**
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Physiology & Human Nervous System: Cell, Bioelectricity, Sodium Potassium pump, Action and Resting potentials, Bioelectric Signals, Nervous System, Peripheral Nervous System, Autonomic Nervous System, SNS, PNS.

Electro-Physiological Measurements: Basic components of biomedical electronics system, Electrodes: Micro, Needle and Surface electrodes, Electrical activity of heart, Generation and Recording of ECG signals, ECG Waves and Time Intervals, Heart Rhythms, Heart beat morphologies, Noise and artifacts, Respiratory system, EEG, EEG Rhythms and waveforms, Recording.

Non-Electrical Parameter Measurement: Blood pressure measurement, Cardiac output, Heart Sounds, Respiratory rate, Gas volume, Flow rate, ph value, ESR, GSR, Plethysmography.

Assistive Restorative and Medical Imaging Equipments: Phonocardiography, Vectrocardiography, Defibrillators, Pacemakers, X-Ray, Ultrasonography, Computer Tomography, MRI.

Texts / References

1. Joseph J. Carr and John M. Brown, "Introduction to Biomedical Equipment Technology" 4th edition, Pearson Education India, 2001.
2. Leslie Cromwell, Fred J, Weibell and Erich A. Pfeiffer, "Biomedical Instrumentation and Measurements" Prentice Hall of India Pvt. Ltd, New Delhi.
3. John G. Webster (Ed.), "Medical Instrumentation Application & Design" 3rd Edition, Wiley India.
4. Khandpur R S, "Handbook on Biomedical Instrumentation" TMH, 13th Reprint, New Delhi.
5. Barbara Christe, "Introduction to Biomedical Instrumentation: The Technology of Patient Care" Cambridge University Press 2009.

MTVL-311 Hardware-Software Co-design

	L	T	P
Internal Marks:50			
External Marks: 100	**3**	**1**	**0**
Total Marks:150			

Introduction: Motivation hardware & software co-design, system design consideration, research scope & overviews.

Hardware Software back ground: Embedded systems, models of design representation, the virtual machine hierarchy, the performance3 modeling, Hardware Software development.

Hardware Software co-design research: An informal view of co-design, Hardware Software tradeoffs, crosses fertilization, typical co-design process, co-design environments, limitation of existing approaches, ADEPT modeling environment.

Co-Design concepts: Functions, functional decomposition, virtual machines, Hardware Software partitioning, Hardware Software partitions, Hardware Software alterations, Hardware Software tradeoffs, co-design.

Methodology for co-design: Amount of unification, general consideration & basic philosophies, a framework for co-design.

Unified representation for Hardware & Software: Benefits of unified representation, modeling concepts.

An abstract Hardware & Software model: Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model.

Performance evaluation: Application of the abstract Hardware & Software model, examples of performance evaluation.

Texts / References

1. Sanjaya Kumar, James H. Ayler "The Co-design of Embedded Systems: A Unified Hardware Software Representation" Kluwer Academic Publisher, 2002.
2. Gomaa, "Software Design Methods for Concurrent and Real-time Systems" AddisonWesley, 1993.
3. H. Kopetz, "Real-time Systems" Kluwer, 1997.
4. R.Gupta, "Co-synthesis of Hardware and Software for Embedded Systems" Kluwer 1995.