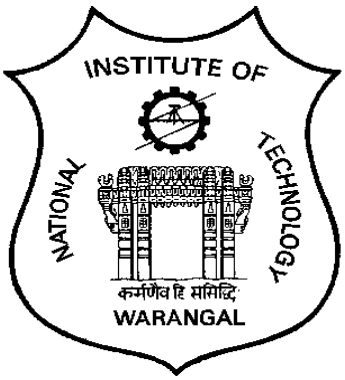
NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL



SCHEME OF INSTRUCTION AND SYLLABI
FOR M.TECH PROGRAMS

Effective from 2014-15

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY WARANGAL

VISION

Towards a Global Knowledge Hub, striving continuously in pursuit of excellence in Education, Research, Entrepreneurship and Technological services to the society

MISSION

- Imparting total quality education to develop innovative, entrepreneurial and ethical future professionals fit for globally competitive environment.
- Allowing stake holders to share our reservoir of experience in education and knowledge for mutual enrichment in the field of technical education.
- Fostering product oriented research for establishing a self-sustaining and wealth creating centre to serve the societal needs.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

Create an Educational environment to prepare the students to meet the challenges of modern electronics and communication Industry through state of art technical knowledge and innovative approaches.

MISSION

- To create learning, Development and testing environment to meet ever challenging needs of the Electronic Industry.
- To create entrepreneurial environment and industry interaction for mutual benefit.
- To be a global partner in training human resources in the field of chip design, instrumentation and networking.
- To associate with international reputed institution for academic excellence and collaborative research.

M.TECH ELECTRONICS AND COMMUNICATION ENGINEERING

SPECIALIZATION: VLSI System Design

SCHEME AND SYLLABI

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY

WARANGAL

COURSE CURRICULUM FOR THE M.TECH PROGRAMME IN

VLSI SYSTEM DESIGN

Graduate Attributes

These Graduate Attributes are identified by National Board of Accreditation.

1. Scholarship of Knowledge: Acquire in-depth knowledge of specific discipline or professional area, including wider and global perspective, with an ability to discriminate, evaluate, analyze and synthesize existing and new knowledge, and integration of the same for enhancement of knowledge.

2. Critical Thinking: Analyze complex engineering problems critically, apply independent judgment for synthesizing information to make intellectual and/or creative advances for conducting research in a wider theoretical, practical and policy context.

3. Problem Solving: Think laterally and originally, conceptualize and solve engineering problems, evaluate a wide range of potential solutions for those problems and arrive at feasible, optimal solutions after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise.

4.Research Skill: Extract information pertinent to unfamiliar problems through literature survey and experiments, apply appropriate research methodologies, techniques and tools, design, conduct experiments, analyze and interpret data, demonstrate higher order skill and view things in a broader perspective, contribute individually/in group(s) to the development of scientific/technological knowledge in one or more domains of engineering.

5. Usage of modern tools: Create, select, learn and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modeling, to complex engineering activities with an understanding of the limitations.

6. Collaborative and Multidisciplinary work: Possess knowledge and understanding of group dynamics, recognize opportunities and contribute positively to collaborative-multidisciplinary scientific research, demonstrate a capacity for self-management and teamwork, decision-making based on open-mindedness, objectivity and rational analysis in order to achieve common goals and further the learning of themselves as well as others.

7. Project Management and Finance: Demonstrate knowledge and understanding of engineering and management principles and apply the same to one's own work, as a member and leader in a team, manage projects efficiently in respective disciplines and multidisciplinary environments after consideration of economic and financial factors.

8.Communication: Communicate with the engineering community, and with society at large, regarding complex engineering activities confidently and effectively, such as, being able to comprehend and write effective reports and design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.

9. Life-long Learning: Recognize the need for, and have the preparation and ability to engage in life-long learning independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.

10. Ethical Practices and Social Responsibility: Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

11. Independent and Reflective Learning: Observe and examine critically the outcomes of one's actions and make corrective measures subsequently, and learn from mistakes without depending on external feedback.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.TECH IN VLSI-SYSTEM DESIGN

Program Education Objectives

PEO 1	Design and generate GDS files for digital, analog and mixed signal integrated circuits using appropriate EDA tools, computational techniques, algorithms and develop testing methods.
PEO 2	Model passive and active devices suiting advances in IC fabrication technology.
PEO 3	Design low power and improved performance VLSI signal processing architectures and implement them on FPGA platforms.
PEO 4	Communicate effectively and convey ideas using innovative engineering tools.
PEO 5	Perceive lifelong learning as a means of enhancing knowledge base and skills necessary to contribute to the improvement of their profession and community.

Mapping of Mission statements with program educational objectives

Mission	PEO1	PEO2	PEO3	PE04	PEO5
To create learning, development and testing environment to meet ever challenging needs of the Electronic industry.	3	3	3	2	2
To create entrepreneurial environment and industry interaction for mutual benefit.	2	2	2	3	3
To be a global partner in Training the human resource in the fields of Chip Design, Instrumentation and Networking.	2	3	2	2	3
To associate with internationally reputed Institutions for academic excellence and collaborative research.	2	2	2	2	3

Mapping of program educational objectives with graduate attributes

PEO	GA 1	GA 2	GA 3	GA 4	GA 5	GA 6	GA 7	GA 8	GA 9	GA1 0	GA1 1	GA1 2
PEO 1	3	2	-	2	-	-	1	3	-	2	-	2
PEO 2	3	1	-	1	-	1	2	3	-	2	2	2
PEO 3	2	1	3	3	3	2	3	3	2	2	3	2

PEO 4	3	3	2	-	3	2	3	3	3	3	3	3
PEO 5	2	2	3	3	3	-	-	3	-	2	-	2

Program Outcomes

PO1	Identify, characterize, model and offer solutions to issues related to IC design
PO2	Understand the advances in the VLSI technologies
PO3	Identify design requirements of analog and mixed signal circuits
PO4	Design low power digital integrated circuits
PO5	Develop efficient architectures for improving system performance in terms of speed, power consumption, and accuracy.
PO6	Perform all design functions using EDA tools.
PO7	Specify appropriate physical design automation algorithm meeting system requirements.
PO8	Develop test strategies suitable for the integrated circuits in analog and mixed signal domain.
PO9	Communicate technical material through formal written reports satisfying accepted standards of writing style while adopting professional ethics
PO10	Work in a team effectively with improved communication skills.
PO11	Understand how organizations work, generate wealth, manage finances and effectively utilize human resources.
PO12	Develop lifelong learning methods.

Mapping of POs and PEOs

	PEO1	**PEO2**	**PEO3**	**PEO4**	**PEO5**
PO1	3	3	2	1	2
PO2	2	3	2	1	2
PO3	3	2	2	1	2
PO4	2	2	3	1	2
PO5	2	2	3	1	2
PO6	3	1	1	1	2
PO7	3	1	2	1	2
PO8	3	3	1	1	2
PO9	1	1	1	3	2

PO10				3	2
PO11				3	
PO12	1	1	1	2	3

Detailed Course Structure

I Year-I Sem						
S.No	**Course No**	**Course Name**	**L**	**T**	**P**	**C**
1	MA5017	Computational Techniques in Microelectronics	3	0	0	3
2	EC5201	Device Modelling	3	0	0	3
3	EC5202	Digital IC Design	4	0	0	4
4	EC5203	Analog IC Design	4	0	0	4
5		Elective - I	3	0	0	3
6		Elective - II	3	0	0	3
7	EC5204	Analog IC Design Laboratory	0	0	6	4
8	EC5205	Digital IC Design Laboratory	0	0	3	2
Total			**20**	**0**	**9**	**26**
I Year-II Sem						
S.No	**Course No**	**Course Name**	**L**	**T**	**P**	**C**
1	EC5251	Testing and Testability	3	0	0	3
2	EC5252	Mixed Signal Design	4	0	0	4
3	EC5253	RF IC Design	3	0	0	3
4		Elective - III	3	0	0	3
5		Elective - IV	3	0	0	3
6		Elective - V	3	0	0	3
7	EC5254	Mixed Signal Design Laboratory	0	0	6	4
8	EC5255	Physical Design Automation Laboratory	0	0	3	2
9	EC5291	Seminar	0	0	3	2
Total			**19**	**0**	**12**	**27**
II Year-I Sem						
S.No	**Course No**	**Course Name**	**L**	**T**	**P**	**C**
1	EC6241	Comprehensive Viva-voce	0	0	0	4

2	EC6249	Dissertation Part-A	0	0	0	8
Total			**0**	**0**	**0**	**12**
II Year-II Sem						
S.No	**Course No**	**Course Name**	**L**	**T**	**P**	**C**
1	EC6299	Dissertation Part-B	0	0	0	18
Total			**0**	**0**	**0**	**18**

List of Electives

S.No	**Cour No**	**Course Name**	**L**	**T**	**P**	**C**
Elective - I	EC5211	Microchip Fabrication Techniques	3	0	0	3
	EC5212	Clean room Technology and Maintenance	3	0	0	3
	EC5213	ULSI Technology	3	0	0	3
Elective - II	EC5214	VLSI DSP Architectures	3	0	0	3
	EC5215	Hardware/Software Co-design	3	0	0	3
	EC5216	Hardware Description Languages	3	0	0	3
Elective - III	EC5261	FPGA Design	3	0	0	3
	EC5262	Full Custom Design	3	0	0	3
	EC5263	ASIC System Design	3	0	0	3
Elective - IV	EC5264	Low Power VLSI Design	3	0	0	3
	EC5265	Ga As Technology	3	0	0	3
	EC5266	Formal Verification	3	0	0	3
Elective - V	EC5267	CAD for VLSI	3	0	0	3
	EC5268	MEMS & Microsystems	3	0	0	3
	EC5269	Physical Design Automation	3	0	0	3

Credit Structure					
Category	**I SEM**	**II SEM**	**III SEM**	**IV SEM**	**Total**
Core courses	14	10	0	0	24
Electives	6	9	0	0	15
Lab Courses	6	6	0	0	12
Comprehensive Viva-Voce	0	0	4	0	4
Seminar	0	2	0	0	2
Project	0	0	8	18	26
Total	**26**	**27**	**12**	**18**	**83**

MA5017	Computational Techniques in Microelectronics	PCC	3 – 0 – 0	3 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Formulate problem in terms of finite element
CO2	Estimate the error in the method he uses
CO3	Generate the grid required for the problem
CO4	Apply FEM, FVM methods to analyse ICs.

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	1	1	2	1						1
CO2		1	2	1		2	2					1
CO3		3	1	1	1	1						2
CO4				1			1					1

Detailed syllabus

Numerical solution of differential equations: FEM, FVM, FDM. Linear circuit simulation techniques: Forward Euler Approximation, Backward Euler Approximation, Trapezoidal Approximation, One Step Integration Approximation

Non-linear circuit simulation techniques: Non Linear DC analysis, Newton RaphsonIteration, Multi-Dimensional Newton RaphsonIteration. Error estimates, Transient and small signal solutions, Applications to device and process simulation, Layout algorithms, Yield estimation algorithms, Symbolic analysis and Synthesis of Analog ICs.

Introduction to physical design : VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles.

Reading:

1. L.O.Chua and P.M.Lin, Computer Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques, Prentice Hall, 1975.

Reference:

1. Pallage, R.Rohrer and C.Visweswaraiah, Electronic Circuit and System Simulation Methods, McGrawHill, 1995.
2. NaveedShewani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.

EC5201	Device Modeling	PCC	3 – 0 – 0	3 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Formulate problem sin terms of finite elements
CO2	Develop solution to overcome short channel issues.
CO3	Develop compact models appropriate for industry
CO4	Analyze current distribution in the devices like transistors, MOS devices

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	2	1	1	3						3
CO2	2	3	1	1	1	2						2
CO3	2	3	2	2	1	1						3
CO4	1	2	1	1	1	1						3

Detailed syllabus

Basic Device Physics: Energy bands in solids , p-n Junctions, MOS Capacitors, Metal-Silicon Effects, MOSFET Devices Design: Long Channel MOSFET, Short-Channel MOSFETS, MOSFET Scaling, Threshold Voltage. MOSFET DC Model: Drain Current Calculations, Pao-Sah Model, Charge Sheet Model, Piece-Wise Drain Current Model for Enhancement Devices

CMOS Performance Factors: Basic CMOS Circuit Elements, Parasitic Elements, Sensitivity of CMOS delay to device parameters, Performance Factors of Advanced CMOS Devices.

Bipolar Devices Design: npn&pnp Transistors, Ideal Current-Voltage Characteristics, Bipolar Device Models for Circuit and Time-Dependent Analyses, Modern Bipolar Transistor Structures, Figures of Merit of a Bipolar Transistors, Digital Bipolar Circuits

MOSFET DC Model: Drain Current Calculations, Pao-Sah Model, Charge Sheet Model, Piece-Wise Drain Current Model for Enhancement Devices.

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Reading:

1. M.S. Tyagi, Introduction to Semiconductor Materials and Devices, Wiley, 2008.
2. Ben G Streetman, Solid State Electronic Devices, 6th Edition, Pearson Prentice-Hall, 2009.

3. Yuan Taur and T H Ning, Fundamentals of Modern VLSI Devices, 2nd Edition, Cambridge

EC5202	Digital IC Design	PCC	4 – 0 – 0	4 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Design CMOS inverters with specified noise margin and propagation delay.
CO2	Synthesize digital circuit using Verilog HDL.
CO3	Implement efficient techniques at circuit level for improving power and speed of combinational and sequential circuits
CO4	Design a processor meeting timing constraints.
CO5	Design memories with efficient architectures to improve access times, power consumption.

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	2	3	2							1
CO2	2	1	1	1	2	2	1					
CO3	2	1	1	2	3	1		1				1
CO4	1	1	2	2	2	1	2	1				
CO5	1	1	1	2	3			1				

Detailed syllabus

MOS INVERTERS: Introduction, Definitions and Properties, Static CMOS Inverter, Static and Dynamic Power Dissipation, CMOS inverter delay time definitions and calculations

DESIGNING COMBINATIONAL LOGIC GATES in CMOS: Introduction, Static CMOS Design, Dynamic CMOS Design, Power Consumption in CMOS Gates.

DESIGNING SEQUENTIAL LOGIC GATES in CMOS: Introduction, Static Sequential Circuits Dynamic Sequential Circuits, Non-Bistable Sequential Circuits, Logic Style for Pipelined Structures.Timing Issues in Digital Circuits**:** Introduction, Clock Skew and Sequential Circuit Performance, Clock Generation and Synchronization.

DESIGNING ARITHMETIC BUILDING BLOCKS: Introduction**,** The Adder: Definition, Circuit and Logic Design, The Multiplier: Definition**,** The Shifter: Definition**,** Power Considerations in Data path Structures.Designing Memory **:**Introduction, Semiconductor Memories - An Introduction, The Memory Core: RAM, ROM**,**Memory Peripheral Circuitry

Reading:
1. Jan M Rabaey, Digital Integrated Circuits, 2nd Edition, Pearson Education, 2003.
2. Sung-Mo Kang, CMOS Digital Integrated Circuits, 3rd Edition, McGraw-Hill, 2003.

EC5203	ANALOG IC DESIGN	PCC	4 – 0 – 0	4 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the significance of different biasing styles and apply them aptly for different circuits.
CO2	Design basic building blocks like sources, sinks, mirrors, up to layout level.
CO3	Comprehend the stability issues of the systems and design OpAmp fullycompensated against process, supply and temperature variations.
CO4	Identify suitable topologies of the constituent sub systems and corresponding circuits as per the specifications of the system
CO5	Design Analog integrated system including parasitic effects upto tape-out

Mapping of course outcomes with program outcomes:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	3		2	1		1				3
CO2	2	1	3		2	2		1				2
CO3	2	1	3		2	1						
CO4	1	1	3		3	2						
CO5	1	1	3		2	1						2

Detailed syllabus
MOS FET device I/V characteristics, second order effects, Capacitances, body bias effect, Biasing Styles, MOS small signal Model, NMOS verses PMOS devices.

Basic building blocks and basic cells-Switches, active resistors, Current sources and sinks, Current mirrors: Basic current mirror, cascode current mirror, low voltage current mirror, Wilson and Widlar current mirrors, voltage and current references, Single stage amplifier: Common source stage with resistive load, diode connected load, triode load, CS stage with source degeneration, source follower, CG stage, Gain boosting techniques, Cascode, folded cascode, choice of device models.

Differential amplifier: Quasi differential amplifier, significance of tail current source, errors due to mismatch, replication principle, qualitative analysis, common mode response, differential amplifier with MOS loads, single ended conversion, gilbert cell. Operational amplifier-characterization, 2 stage OP amp, process and temperature independent compensation, output stage.

Band Gap Reference: General considerations, Supply independent biasing, temperature-independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT generation, constant g_m biasing, speed and noise issues, case study, curvature correction. PTAT, CTAT, Bandgap circuit, start-up circuit, curvature correction Design.

Reading:

1. P R Gray and R G Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2. Mohammed Ismail and Terri Fiez, Analog VLSI: Signal and Information Processing, McGraw-Hill, 1994.
3. Geiger, Allen and Stradder, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 2010.

EC5211	MICROCHIP FABRICATION TECHNIQUES	DEC	3 – 0– 0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Comprehend impact of semiconductor industry on the design and development of integrated system
CO2	Acquaint with clean room technology
CO3	Understand oxidation methods, aspects of photolithography diffusion, ion implantation and deposi techniques
CO4	Specify NMOS and CMOS design rules corresponding to 180nm, 90nm, 45 nm technologies
CO5	Understand packaging principles

Mapping of course outcomes with program outcomes

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5211 MFT	CO1	1	2		1			1					1
	CO2	1	1										1
	CO3	1	1		1		1	1					
	CO4	2	2	1	1								1
	CO5	1	1										

Detailed syllabus

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization.

Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping, Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitoxy, molecular beam epitaxy.

Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors, Packaging: Chip characteristics, package functions, package operations

Reading:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000
3. Eugene D. Fabricius, Introduction to VLSI design, McGraw Hill, 1999
4. Wani-Kai Chen (editor), The VLSI Hand book, CRI/IEEE press, 2000
5. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994

6. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY, 1988

7. N.B. Chakrabarti, Introduction to Integrated Circuit Logic and Memory, Oxford and IBH, 1999

EC5212	Clean Room Technology and Maintenance	DEC	3 – 0– 0	3 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Specify cleanroom standards and ancillary cleanrooms.
CO2	Identify fabrication materials and surface finishes.
CO3	Analyze air quantities, pressure differences and clean room disciplines

Mapping of course outcomes with program outcomes

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5212 CTM	CO1	1	1			3							1
	CO2	1	1		3								
	CO3			2									1

Detailed syllabus

Introduction, Cleanroom Classification Standards, Unidirectional air flow cleanroom, Basis of Clean room standards, Federal Standards 209 ,ISO standard 14644-1:1999,Cleanroom classification(Pharmaceutical, cleanrooms)

Design of Turbulently Ventilated and Ancillary Cleanrooms, Mini environments, isolators and RABS, Containment zone, Construction and clean build, Design of Unidirectional Cleanrooms.

High Efficiency Air filtration, Particle removal mechanisms, Testing of high efficiency filters.

Cleanroom Testing and Monitoring, Principles of cleanroom testing, Testing in relation to room type and occupation state, Monitoring of cleanroom.

Measurement of Air Quantities and Pressure Differences, Air movement control, Recovery test methods, Cleanroom containment leak testing.

Filter Installation leak testing, Operating a clean room, Materials, equipment and machinery, Clothing, masks and gloves, Cleaning a cleanroom.

Reading:

1. William White, Cleanroom Technology: Fundamentals of Design, Testing and Operation, 2nd Edition, Wiley, 2010.
2. Matts Ramstorp, Introduction to Contamination Control and Cleanroom Technology, Wiley, 2008.
3. Wani-Kai Chen (editor), The VLSI Hand book, CRI/IEEE press, 2000

EC5213	ULSI Technology	DEC	3 – 0– 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand transmission electron microscopy.
CO2	Apply the concept of Metallization, interconnects, Process integration.
CO3	Understand fabrication issues of ULSI devices

Mapping of course outcomes with program outcomes

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5213 UT	CO1	1	1		1	1	1						1
	CO2	1	1										1
	CO3	2	2		1		1						

Detailed syllabus

Microelectronics and microscopy,ULSI process technology,Application of TEM for construction analysis,TEM sample preparation techniques.

Ion implantation and substrate defects,Dielectrics and isolation,Silicides, polycide and salicide,Metallization and interconnects.

TEM in failure analysis,Novel devices and materials,TEM in under bump metallization and advanced electronics packaging technologies,High – resolution TEM in microelectronics.

ULSI devices I: DRAM cell with planar capacitor,ULSI devices II: DRAM cell with stacked capacitor ,ULSI devices III: DRAM cell with trench capacitor,ULSI devices IV: SRAM.

Reading:

1. C. Y. Chang, S.M. Sze, ULSI Technology, McGraw-Hill, 2000.

2. Chih-Hang Tung, George T.T. Sheng, Chih-Yuan Lu, ULSI Semiconductor ProcessTechnology Atlas, John Wiley & Sons, 2003.

EC5214	VLSI DSP ARCHITECTURES	DEC	3 – 0– 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Architect programmable DSP devices optimizing the performance.
CO2	Design efficient architectures, algorithms and circuits improving size, power consumption, and speed and round-off noise.
CO3	Translate effective algorithm design to integrated circuit implementations.
C04	Comprehend various sources of errors in implementation of DSP algorithms and device means to control them while implementing the DSP systems as per the specifications demanded by applications.

Mapping of course outcomes with program outcomes

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5214 VLSI DSP ARCH	CO1	2	2	1	1	2	1						1
	CO2	2	2	1	3	3	1	1					1
	CO3	2	1		2	2							
	CO4	3	1		2	2							2

Detailed syllabus

Essential features of Instruction set architectures of CISC, RISC and DSP processors and their implications for Implementation as VLSI Chips, Micro programming approaches for implementation of control part of the processor.Assessing understanding performance: Introduction, CPU performance and its factors, evaluating performance, real stuff: Two spec bench marks and performance of recent INTEL processors, fallacies and pitfalls.

Data path and control: Introduction, logic design conventions, building a data path, a simple implementation scheme, a multi cycle implementation, exceptions, micro programming: simplifying control design, an introduction to digital design using hardware description language, fallacies and pitfalls.

Enhancing performance with pipelining: An overview of pipelining, a pipe lined data path, pipe lined control, data hazards and forwarding, data hazards and stalls, branch hazards, using a hard ware description language to describe and model a pipe line, exceptions, advanced pipelining: extracting more performance, fallacies and pitfalls

Computational accuracy in DSP implementations: Introduction, number formats for signals and coefficients in DSP systems, dynamic range and precision, sources of errors in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors.

Architectures for programmable digital signal processing devices: introduction, basic architectural features, DSP computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

Reading:

1. D.A, Patterson And J.L. Hennessy, Computer Organization and Design: Hardware / Software Interface, 4th Edition, Elsevier, 2011.
2. A.S. Tannenbaum, Structured Computer Organization, 4th Edition, Prentice-Hall, 1999
3. W. Wolf, Modern VLSI Design: Systems on Silicon, 2nd Edition, Pearson Education, 1998
4. KeshabParhi, VLSI digital signal processing systems design and implementations, Wiley 1999
5. Avatar sigh, Srinivasan S, Digital signal processing implementations using DSP microprocessors with examples, Thomson 4th reprint, 2004.

EC5215	**Hardware / Software Co-Design**	**DEC**	**3 – 0– 0**	**3 Credits**

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand Serial and parallel communication protocols.
CO2	Model data flow and implement the same through software and hardware
CO3	Operate data flow using USB and CAN bus for PIC microcontrollers.
CO4	Design embedded Ethernet for Rabbit processors.
C05	Design CORDIC and Crypto coprocessor

Mapping of course outcomes with program outcomes

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5215 H/SD	CO1			1				2					1
	CO2						1						
	CO3	1	1					3					1
	CO4			2			1						
	CO5		1					1					

Detailed syllabus

The Nature of Hardware and Software: Introducing Hardware/Software Co-design, The Quest for Energy Efficiency, The Driving Factors in Hardware/Software Co-design, The Dualism of Hardware Design and Software Design. Data Flow Modeling and Transformation: Introducing Data Flow Graphs, Analyzing Synchronous Data Flow Graphs, Control Flow Modeling and the Limitations of Data Flow, Transformations.

Data Flow Implementation in Software and Hardware: Software Implementation of Data Flow, Hardware Implementation of Data Flow, Hardware/Software Implementation of Data Flow.

Analysis of Control Flow and Data Flow: Data and Control Edges of a C Program, Implementing Data and Control Edges, Construction of the Control Flow Graph4.4 Modern Bipolar, Transistor Structures, Construction of the Data Flow Graph.

Finite State Machine with Datapath: Cycle-Based Bit-Parallel Hardware, Hardware Modules, Finite State Machines with Datapath, FSMD Design Example: A Median Processor

System on Chip: The System-on-Chip Concept, Four Design Principles in SoC Architecture, SoC Modeling in GEZEL. Applications: Trivium Crypto-Coprocessor, CORDIC Co-Processor.

Reading:

1. Patrick Schaumont, A Practical Introduction to Hardware/Software Co-design, Springer, 2010.
2. Ralf Niemann, Hardware/Software Co-Design for Data flow Dominated Embedded Systems, Springer, 1998.

EC5216	Hardware Description Languages	DEC	3 – 0– 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Differentiate sequential language and concurrent language
CO2	Design combinational logic circuits using VHDL.
CO3	Design sequential logic circuits using VHDL.
CO4	Model Analog circuits using Verilog AMS.
CO5	Differentiate sequential language and concurrent language

Mapping of course outcomes with program outcomes

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5216 HDL	CO1		2	2	1	2							1
	CO2	1	1	1	1	3							1
	CO3	1	1	1	1	2							
	CO4	2	2	2	1	1							1

Detailed syllabus

Introduction: About VHDL, Design Flows & EDA Tools, Code Structure, Data types, Operators and Attributes: Operators, Attributes, User-Defined Attributes, Operator, overloading

Concurrent Code: Concurrent versus Sequential, Using Operators, WHEN, Generate and Block, Sequential Code: Process, Signals and Variables, IF, WAIT, CASE, Using Sequential, Code To Design Combinational Circuits

State Machines: Introduction, Design Style #1, Design Style #2 (Stored Output), Encoding Style: From Binary to OneHot

Introduction to Verilog-AMS: Verilog Family of Languages, Mixed Signal Simulators, Applications of Verilog-AMS, Analog Modeling. Language Reference: Basics, Data Types, Signals, Expressions, Analog Behavior

Reading:

1.Volnei A. Pedroni, Circuit Design and Simulation with VHDL, 2nd Edition, MIT Press, 2010.

2. Kenneth S Kundert, Olaf Zinke, Designers Guide to Verilog AMS, Springer, 2004

EC5204	ANALOG IC DESIGN LAB	PCC	0 – 0 – 6	4 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the significance of different biasing styles and apply them aptly for different circuits.
CO2	Design all basic building blocks like sources, sinks, mirrors, up to layout level.
CO3	Comprehend the stability issues of the systems and should be able to design OpAmp fully. Compensated against process, supply and temperature variations.
CO4	Identify the suitable different topologies of the constituent sub systems and corresponding circuits as per the specifications of the system
CO5	Design Analog integrated system completely upto tape-out including parasitic effects

Mapping of COs with POs

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5204 AICD Lab	CO1	2	0	3	0	0	2	0	0	2			2
	CO2	2	0	2	0	0	2						
	CO3	1	1	2			2			1			2
	CO4	1		2			1				2		1
	CO5	1	1	3			3					2	2

Detailed syllabus

Cycle 1:

Lambda calculation for PMOS & NMOS, F_T calculation, Tranconductance plots, Single transistor amplifier, Ideal current source, PMOS current source, NMOS saturated load, Degenerative resistor, Cascade amplifier: Ideal current source, PMOS current source.

Cycle 2:

Current sinks: Basic current sink, Current sink with negative feedback, Bootstrap current sink, Cascode current sink, Regulated cascode current sink.

Current sources: Basic current source, Current source with negative feedback, Bootstrap current source, Cascade current source, Regulated cascade current source,

Current mirrors: Basic current mirror, Wilson current mirror, Cascode current mirror, Regulated cascade current mirror, Widlar current source

Differential amplifier, Two stage Operational amplifier design

Reading:

1) Pr Gray and Rg Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2) Mohammed Ismail and Terri Fiez, Analog VLSI: Signal and Information Processing, McGraw-Hill, 1994.
3) Geiger, Allen and Stradder, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-HillEducation,2010.

EC5205	Digital IC Design Laboratory	PCC	0 – 0 – 3	2 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Design synchronous and Asynchronous sequential circuits using Verilog HDL/ VHDL
CO2	Develop soft methods for identifying faulty digital circuits for the DUT
CO3	Synthesize digital circuit using Verilog HDL/ VHDL
CO4	Design combinational and sequential circuits at circuit level using Tanner tools
CO5	Implement efficient techniques at circuit level for improving power and speed of combinational and sequential circuits using Tanner EDA tool.

Mapping of COs with POs

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5205 DICD Lab	CO1	2	1		1	2	1			2			1
	CO2	2	1		2	1	1		3	2			1
	CO3											2	
	CO4	1			2	3	2						1
	CO5	1	1		3	1	1			2	2		1

Detailed Syllabus:

Module 1: CMOS inverters -static and dynamic characteristics, CMOS NAND, NOR and XOR Gates

Module 2: Static and Dynamic CMOS design- Domino and NORA logic – combinational and sequential circuits, Method of Logical Effort for transistor sizing –power consumption in CMOS gates- Low power CMOS design

Module 3: Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifter –CMOS memory design - SRAM and DRAM

Module 4: Bipolar gate Design- BiCMOS logic - static and dynamic behaviour –Delay and power consumption in BiCMOS Logic.

Module 5: Design and simulation of 32 bits MIPS processor

Reading:

1. Jan M Rabaey, Digital Integrated Circuits, 2nd Edition, Pearson Education, 2003.

2. Sung-Mo Kang, CMOS Digital Integrated Circuits, 3rd Edition, McGraw-Hill, 2003.

EC5251	Testing and Testability	PCC	3 – 0– 0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Identify the significance of testable design
CO2	Understand the concept of yield and identify the parameters influencing the same.
CO3	Specify fabrication defects, errors and faults.
CO4	Implement combinational and sequential circuit test generation algorithms
CO5	Identify techniques to improve fault coverage.

Mapping of course outcomes with program outcomes

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5251 TTY	CO1	1	2	2	2	1			2				1
	CO2	1	3	1	2	2		1	2				
	CO3	2	2	1	2	2		1	2				2
	CO4	1	1	1	1	2	2	1	3				
	CO5	1	1	1	2	2	2		3				2

Detailed syllabus

Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models

Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits. Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms. Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods

Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain based testing method. D-algorithm procedure, Problems, PODEM Algorithm, Problems on PODEM Algorithm. FAN Algorithm, Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan based design.

Classical scan based design, System level DFT approaches, Test pattern generation for BIST, Circular BIST, BIST Architectures, and Testable memory design-Test algorithms-Test generation for Embedded RAMs.

Reading:

1 M. Abramovici, M. Breuer, and A. Friedman, “Digital Systems Testing and Testable Design, IEEE Press, 1990.

Reference Books:

1. Stroud, “A Designer’s Guide to Built-in Self-Test”, Kluwer Academic Publishers, 2002
2. M. Bushnell and V. Agrawal, “Essentials of Electronic Testing forDigital, Memory & Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2000
3. V. Agrawal and S.C. Seth, Test Generation for VLSI Chips, Computer Society Press.1989.

EC5252	Mixed Signal Design	PCC	4 – 0– 0	4 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Should be able to demonstrate corresponding layout techniques with least interference among digital and analog subsystems.
CO2	Should be in a position to design basic cells like OpAmp compensated and high ting against process and temperature variations meeting the mixed signal specifications
CO3	Should be able to design comparators that can meet the high speed requirements of digital circuitry.
C04	Should be able to design a complete mixed signal system that includes efficient data conversion and RF circuits with minimizing switching and phase noise, jitter.

Mapping of course outcomes with program outcomes

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5252 MSD	CO1	1	1	1		1							1
	CO2	1	1	3		1							3
	CO3	1	1	3		3							3
	CO4	1		3		2							
	CO5	1	2			2							2

Detailed syllabus

Simple CMOS Current Mirror, Common-Source Amplifier, Source-Follower, Source-Degenerated Current Mirrors, cascode Current Mirrors, MOS Differential Pair and Gain StageProcess and temperature independent compensation, Ahuza's compensation, nested miller compensation, dynamic offset cancellation techniques. Basic Building Blocks, OpAmp, Capacitors, Switches, Non-overlapping Clocks, Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator , Parasitic-Insensitive Integrators, Signal-Flow-Graph Analysis, Noise in Switched-Capacitor Circuit

Performance of Sample-and-Hold Circuits, Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Bipolar and BiCMOS Sample-and-Holds, Translinear Gain Cell, Translinear Multiplier, Comparator Specifications Input Offset and Noise , Hysteresis, ,Using an OpAmp for a Comparator, Input-Offset Voltage Errors, Charge-Injection Errors, Making Charge-Injection Signal Independent , Minimizing Errors Due to Charge-Injection, speed of Multi-Stage Comparators, Latched Comparators, Latch-Mode Time Constant, Latch Offset, Examples of CMOS and BiCMOS Comparators, Input-Transistor Charge Trapping, Examples of Bipolar Comparators,

Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Deterministic Approach, Stochastic Approach, Signed Codes, Performance Limitations, Resolution, Offset and Gain Error, Accuracy and Linearity

Integrating Converters, Successive-Approximation Converters, DAC-Based Successive Approximation, Charge-Redistribution A/D, Resistor-Capacitor Hybrid, Speed Estimate for Charge-Redistribution Converters, Error Correction in Successive-Approximation Converters

Multi-Bit Successive-Approximatio**n,** Algorithmic (or Cyclic) A/D Converter, Ratio-Independent Algorithmic Converter, Pipelined A/D Converters, One-Bit-Per-Stage Pipelined Converter,1.5 Bit Per Stage Pipelined Converter, Pipelined Converter Circuits,

Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model , Limitations of the Second-Order Small-Signal Model, PLL Design Example, Jitter and Phase Noise, Period Jitter , P-Cycle Jitter, Adjacent Period Jitter, other Spectral Representations of Jitter, Probability Density Function of Jitter, Ring Oscillators , LC Oscillators , phase Noise of Oscillators, jitter and Phase Noise in PLLS

Reading:

1) David A Johns, Ken Martin: Analog IC design, Wiley 2008.
2) R Gregorian and G C Temes: Analog MOS integrated circuits for signal processing, Wiley 1986
3) Roubik Gregorian: Introduction to CMOS Op-amps and comparators, Wiley, 2008

EC5253	RF IC Design	PCC	3 – 0– 0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the design bottlenecks specific to RF IC design, linearity related issues, ISI
CO2	Identify noise sources, develop noise models for the devices and systems
CO3	Specify noise and interference performance metrics like noise figure, IIP3 and different matching criteria.
C04	Comprehend different multiple access techniques, wireless standards and various transceiver architectures
CO5	Design various constituents' blocks of RF receiver front end.

Mapping of course outcomes with program outcomes

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5253 RF IC DESIGN	CO1	2	1	3		1			1				3
	CO2	2		2		1	1						2
	CO3	1		3		2	1		1				1
	CO4			1		1							3
	CO5	1		2		3							

Detailed syllabus

INTRODUCTION TO RF AND WIRELESS TECHNOLOGY: Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology. BASIC CONCEPTS IN RF DESIGN: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

MULTIPLE ACCESS: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards. TRANSCEIVER ARCHITECTURES: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

AMPLIFIERS, MIXERS AND OSCILLATORS: LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

POWER AMPLIFIERS: General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques

Reading:

1) BehzadRazavi, RF Microelectronics Prentice Hall of India, 2001
2) Thomas H. Lee, The Design of CMOS Radio Integrated Circuits**,** Cambridge University Press.

EC5261	FPGA Design	DEC	3 – 0– 0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand design styles.
CO2	Implement memories, multipliers, shifters, ALU using PLD.
CO3	Synthesize Verilog code for special purpose processor using Vertex, Spartan FPGAs.
C04	Implement parameterized library cell design.

Mapping of course outcomes with program outcomes

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5261 FPGA DESIGN	CO1	2	2	2	1	1							2
	CO2	2	1	2	3	3							1
	CO3	2	1	2	3	2	1	1	1				2
	CO4	3	1	1	2	2							

Detailed syllabus

INTRODUCTION TO FPGAs: Design and implementation of FPGA, Evolution of programmable devices, Application of FPGA.

DEISGN EXAMPLES USING PLDs Design of Universal block, Memory, Floating point multiplier, Barrel shifter.

SPECIAL PURPOSE PROCESSORS Programming technologies, Commercially available FPGAs, Xilinx's Vertex and Spartan, Actel's FPGA, Altera's FLEX 10k.

LOGIC BLOCK ARCHITECTURES

Logic block functionality versus area-efficiency, Logic block area and routing model, Impact of logic block functionality on FPGA performance, Model for measuring delay.

CASE STUDY – ACTEL FPGA

Reading:

1. John V. Old Field, Richrad C. Dorf, Field Programmable Gate Arrays, Wiley, 2008.

2. Michel John Sebastian Smith, Application Specific Integrated Circuits, Addison Wesley Professional, 2008.

3. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, Field Programmable Gate Arrays, 2nd Edition, Springer, 1992.

EC5262	Full Custom Design	DEC	3 – 0– 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand efficient Layout design techniques
CO2	Absorb the process variations into the layout
CO3	Construct guard rings, pad rings suiting mixed signal environment
C04	Design layouts minimizing stress effects

Mapping of course outcomes with program outcomes

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5262 FCD	CO1	1	1	1	1	1	3	3					
	CO2		1		1		2	3	1				1
	CO3	1		2	1	1	3	3	1				1
	CO4		1	1	1		3	3	1				1

Detailed syllabus

Introduction: Schematic fundamentals, Layout design, Introduction to CMOS VLSI manufacturing processes, Layers and connectivity, Process design rules Significance of full custom IC design, layout design flows**.**

Advanced techniques for specialized building blocks Standard cell libraries, Pad cells and Laser fuse cells, Advanced techniques for building blocks, Power grid Clock signals and Interconnect routing.

Interconnect layout design, Special electrical requirements, Layout design techniques to address electrical characteristics.

Layout considerations due to process constraints Large metal via implementations, Step coverage rules, Special design rules, Latch-up and Guard rings, Constructing the pad ring, Minimizing Stress effects.

Proper layout

CAD tools for layout, Planning tools, Layout generation tools, Support tools.

Reading:

1. Dan Clein, CMOS IC Layout Concepts Methodologies and Tools, Newnes, 2000.
2. Ray Alan Hastings, The Art of Analog Layout, 2nd Edition, Prentice Hall, 2006

EC5263	ASIC System Design	DEC	3 – 0– 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Architect ASIC library design
CO2	Develop programmable ASIC logic cells
CO3	Design I/O cells and interconnects
C04	Identify new developments in SOC and low power design.

Mapping of course outcomes with program outcomes

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5263 ASIC	CO1		2			3	1						1
	CO2				2	1	1						1
	CO3	1	1			1	2						
	CO4		2		3	1	1						1

Detailed syllabus

Introduction, Types of ASIC's Design Flow, CMOS Logic**.** ASIC Library Design, Transistor Parasitic Capacitance, Input Slew Rate, Library-Cell Design, Library Architecture. Programmable ASICs, The Antifuse Metal Antifuse, Static RAM, EPROM and EEPROM Technology, Practical Issues.

Programmable ASIC Logic Cells, Actel, Xilinx LCA., XC3000 CLB, XC4000 Logic Block, XC5200 Logic Block, Xilinx CLB Analysis, Logic Expanders. Programmable ASIC I/O Cells, Totem-Pole Output, Mixed-Voltage Systems, Metastability, Xilinx I/O Block. Boundary Scan.

Programmable ASIC Interconnect and Programmable ASIC Design Software. Actel ACT, RC Delay in Antifuse Connections, Xilinx EPLD Logic Synthesis, FPGA Synthesis, Third-party Software, low level design entry, logic synthesis, simulation,

Test and ASIC construction, VHDL, Verilog HDL, Logic Synthesis, Simulation.

Reading:

1. Michel John Sebastian Smith, Application Specific Integrated Circuits, Addison Wesley Professional, 2008.
2. HimanshuBhatnagar, Advanced ASIC Chip Synthesis: Using Synopsys Design Compiler, 2nd Edition, Kluwer Academic, 2001.

EC 5264	Low Power VLSI Design	DEC	3 – 0 – 0	3 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Identify clearly the sources of power consumption in a given VLSI Circuit
CO2	Analyze and estimate dynamic and leakage power components in a DSM VLSI circuit
CO3	Choose different types of SRAMs/ DRAMs for Low power applications
CO4	Design low power arithmetic circuits and systems
CO5	Decide at which level of abstraction it is advantageous to implement low power techniques in a VLSI system design

Mapping of course outcomes with program outcomes

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	-	1	1	-	-	-	-	-	-	-
CO2	1	1	-	1	2	-	-	-	-	-	-	-
CO3	-	2	-	2	3	-	-	-	-	-	-	-
CO4	-	-	-	3	-	-	-	-	-	-	-	-
CO5	-	-	-	1	-	-	-	--	-	-	-	-

Detailed syllabus

Introduction, Sources Of Power Dissipation, Static Power Dissipation, Active Power Dissipation Designing for Low Power, Circuit Techniques For Leakage Power Reduction

Standard Adder Cells, CMOS Adders Architectures, Low Voltage Low Power Design Techniques, Current Mode Adders

Types Of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison

Sources of power dissipation in SRAMs, Low power SRAM circuit techniques, Sources of power dissipation in DRAMs, Low power DRAM circuit techniques

The increased delays of wires, New materials for wires and dielectrics, Design methods taking into account interconnection delays, Cross talk

Basic background on testing, Unsuitable design techniques for safety-critical applications, Low power and safely operating circuits, Case study – A Low power subsystem design

Reading:

1. Kiat Seng Yeo and Kaushik Roy, Low- Voltage, Low-Power VLSI Subsystems, Edition 2009, Tata Mc Graw Hill
2. Soudris D, Piguet C and Goutis C, Designing CMOS Circuits for Low Power, Kluwer Academic Publishers, 2002

Reference Book: Jan Rabaey, Low Power Design Essentials, Springer

EC5265	GaAs Technology	DEC	3 – 0 – 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Identify clearly the sources of power consumption in a given VLSI Circuit
CO2	Analyse and estimate dynamic and leakage power components in a DSM VLSI circuit
CO3	Choose different types of SRAMs/ DRAMs for Low power applications
CO4	Design low power arithmetic circuits and systems

Mapping of course outcomes with program outcomes

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5265 GAT	CO1	2	1		1								
	CO2	1	1		2								1
	CO3	2	1										
	CO4	1	3		1								1

Detailed syllabus

Non-Silicon MOSFET Technology: Introduction, Brief and Non-Comprehensive History of the NSMOSFET, Surface Fermi Level Pinning: The Bane of NSMOSFET, Technology Development

Properties and Trade-Offs of Compound Semiconductor MOSFETs: Simulation Framework, Power-Performance Trade-offs in Binary III-V Materials (GaAs, InAs, InP and InSb) vs. Si and Ge, Power-Performance of Strained Ternary III-V Material (Inx Ga1−xAs), Strained III-V for p-MOSFETs. Device Physics and Performance Potential of III-VField-Effect Transistors: InGaAs HEMTs

Theory of Hfo2-Based High-K Dielectric Gate Stacks: Methodology of DFT Simulations of High-k Oxides on Semiconductor Substrates, DFT Simulations of High-k Oxides on Si/Ge Substrates.

Materials and Technologies for III-V MOSFETs: Introduction, III-V HEMTs for Digital Applications, Challenges for III-V MOSFETs, and Mobility in Buried Quantum Well Channel.

Atomic-Layer Deposited High-k/III-V Metal-Oxide-Semiconductor Devices and Correlated Empirical Model: History and Current, Empirical Model for III-V MOS, Experiments on High-k/III-V MOSFETs, Technology/Circuit Co-Design for III-V FETs.

Electrical and Material Characteristics of Hafnium Oxide with Silicon Interface Passivation on III-V Substrate for Future Scaled CMOS Technology: Introduction, MOSCAPs and MOSFETs on GaAs with Si, SiGe Interface Passivation Layer (IPL), MOSCAPs and MOSFETs on InGaAs with Si IPL, MOSCAPs and Self-Aligned n-channel MOSFETs on InP, Channel Materials with Si IPL.

Reading:

1. Serge Oktyabrsky, Peide D. Ye, Fundamentals of III-V Semiconductor MOSFETs, Springer, 2010.

2. C.Y. Chang, Francis Kai, GaAs High-speed Devices, Physics Technology and Circuit Applications, John Wiley, 1994.

EC 5266	Formal Verification	DEC	3 – 0 – 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Specify the formal verification techniques
CO2	Implement formal test plan process
CO3	Implement simulation based verification
CO4	Model hardware interfaces with concurrency constructs
CO5	Apply IEEE 1850 property specification language and IEEE1800 Verilog assertions

Mapping of course outcomes with program outcomes

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	-	-	1	-	3	-	-	-	-	-	1
CO2	1	-	-	1	-	2	-	-	-	-	-	-
CO3	3	-	1	-	-	3	-	-	-	-	-	-
CO4	1	-	-	-	-	3	-	-	-	-	-	1
CO5	-	1	-	1	-	-	-	--	-	-	-	-

Detailed syllabus

Verification process: Verification plan, Debug Cycle, Simulation and Output data, Test bench development

Current verification techniques: HDL Software simulator, Accelerated simulation, Process Based Accelerator techniques, Hardware emulation, FPGA prototyping

Introduction to formal techniques and property specification: Reachability analysis, Elements of property languages, Property language layers, PSL basics, Formal test plan process

Techniques for proving properties: Abstraction reduction, Compositional reasoning, Counter abstraction, Gradual Exhaustive formal verification

Final system simulation: Module verification, Full simulation from a simulation, Full Simulation from a formal verification

IEEE 1850 PSL Property specifications and IEEE 1800 Verilog assertions: Introduction, operations and keywords, PSL Boolean and temporal layer, Introduction to IEEE 1800 System Verilog, Sequence and property, BNF 185 and BNF 223

Reading:

1. Douglas L Perry Harry D Foster, Applied Formal Verification, McGraw Hill, 2005.
2. William K Lam, Hardware Design Verification: Simulation and Formal Method-based Approaches, Prentice Hall, 2008.

EC5267	CAD for VLSI	DEC	3 – 0 – 0	3 Credits

Pre-requisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Specify layout techniques in IC
CO2	Identify algorithms required for circuit simulators
CO3	Incorporate timing analysis & floor planning
CO4	Apply scripting language PERL to improve EDA tool flow

Mapping of course outcomes with program outcomes

	Course Outcomes	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12
EC5267 CAD	CO1	2	-	-	-	-	2	2	-	-	-	-	-
	CO2	1	-	-	-	-	2	3	-	-	-	-	1
	CO3	1	-	-	-	-	3	1	-	-	-	-	1
	CO4	1	1	-	-	-	2	1	-	-	-	-	-

Detailed syllabus

Introduction to Design Methodologies: The VLSI Design Problem, Design Methods and Technologies, Layout Methodologies, Top-Down Approach: Routing: Fundamentals, Global Routing, Detailed Routing.

Performance Issues in Circuit Layout: Delay Models, Timing Driven Placement, Timing Driven Routing, Power Minimization.

Single-Layer Routing and Applications: Planar Subset Problem, Single-Layer Global Routing, Over-the-cell Routing, Multichip Modules, Wire-Length and Bend Minimization Techniques.

Reading:

1. S.H. Gerez, Algorithms for VLSI Design Automation, Wiley, 2006.

2. M. Sarrafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, McGraw Hill, 1996.

EC 5268	MEMS and Microsystems	DEC	3 – 0 – 0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the products and materials used in MEMS and Micro sensors.
CO2	Use the reconfigurable design implementation in MEMS.
CO3	Apply different bio medical applications

Mapping of course outcomes with program outcomes

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	2	1	1	1	-	-	-	-	-	-	1
CO2	-	1	1	2	3	1	-	-	-	-	-	1
CO3	1	1	-	2	1	-	-	-	-	-	-	1

Detailed syllabus

OVERVIEW OF MEMS AND MICROSYSTEMS: Mems And Microsystems, Evolution of micro fabrication, Microsystems and miniaturization, Application of Microsystems, Markets for Microsystems

WORKING PRINCIPLES OF MICROSYSTEMS: Introduction, MEMS and Micro actuators, Microfluidics, Micro actuators with Mechanical inertia

ENGINEERING SCIENCE FOR MICROSYSTEMS DESIGN: Introduction, Molecular theory of matter and intermolecular forces, Doping of semiconductor, Plasma physics, Electrochemistry

THERMOFLUID ENGINEERING AND MICROSYSTEMS DESIGN: Introduction, Clock Skew and Sequential Circuit Performance, Clock Generation and Synchronization

DESIGNING ARITHMETIC BUILDING BLOCKS: Introduction, Basic equation in continuum fluid dynamics, Laminar fluid flow in circular conduits, Computational fluid dynamics, incompressible fluid flow in micro-conduits

MICROSYSTEMS FABRICATION PROCESSES: Introduction, Photolithography, Diffusion, Oxidation, Chemical vapour deposition

Reading:

1. Tai-Ran Hsu, MEMS and Microsystems, 2nd Edition, Wiley, 2008.

2. Mohamad Gad El Hak, MEMS Design and Fabrication, 2nd Edition, CRC Press, 2006.

EC5269	Physical Design Automation	DEC	3 – 0 – 0	3 Credits

Prerequisites: None

Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the relationship between design automation algorithms and variousconstraints posed by VLSI fabrication and design technology.
CO2	Adapt the design algorithms to meet the critical design parameters
CO3	Identify layout optimization techniques and map them to the algorithms
CO4	Develop proto-type EDA tool and test its efficacy.

Mapping of course outcomes with program outcomes

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	-	-	1	1	3	2	-	-	-	-	1
CO2	2	-	-	1	-	2	3	-	-	-	-	-
CO3	1	-	-	1	-	3	2	-	-	-	-	1
CO4	1	-	-	-	1	2	2	-	-	-	-	1

Detailed syllabus

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi chip modules.

Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbor pointers, corner stitching, multi-layer operations,

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circle graphs

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms

Reading:

1) 1NaveedShervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2) Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008

EC5254	MIXED SIGNAL DESIGN LAB	PCC	0 – 0 – 6	4 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Understand the necessity of mixed signal systems
CO2	Implement layout techniques specific to mixed signal IC design with least interference among digital and analog subsystems.
CO3	Design OPamp compensated against process and temperature variations meeting the mixed signal specifications
CO4	Design comparators that can meet the high speed requirements of digital circuitry.
CO5	Design a complete mixed signal system that includes efficient data conversion and RF circuits with minimizing switching and phase noise, jitter.

Mapping of COs with POs

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5254 MSD Lab	**CO1**	**1**	1	3	1	**1**	**2**			2		2	**1**
	CO2		1	3	1		**3**			2			**1**
	CO3			2	1	**1**	**1**			2			**1**
	CO4		1	2	1		**1**			2	2		**1**
	CO5	**1**	1	3			**2**			2		2	**1**

Detailed Syllabus:

Cycle 1:

1) Fully compensated op-amp with resistor and miller compensation
2) High speed comparator design
   i. Two stage cross coupled clamped comparator
   ii. Strobed Flip-flop
3) Data converter

Cycle 2:

1) Switched capacitor circuits
   i. Parasitic sensitive integrator
   ii. Parasitic insensitive integrator
2) Design of PLL
3) Design of VCO
4) Bandgap reference circuit
5) Layouts of All the circuits Designed and Simulated

Reading:

1) David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2) R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processsing, Wiley, 1986.
3) Roubik Gregorian, Introduction to CMOS OpAmp and Comparators, Wiley, 1999.
4) Alan Hastlings, The art of Analog Layout, Wiley, 2005.

EC5255	Physical Design Automation Lab	PCC	0 – 0 – 6	4 Credits

Prerequisites: None
Course Outcomes: At the end of the course the student will be able to:

CO1	Apply the constraints posed by the VLSI fabrication technology to design automation tools.
CO2	Adapt the design algorithms to meet the critical design parameters
CO3	Simulate layout optimization techniques and map them to the algorithms
CO4	Develop proto-type EDA tool and test its efficacy.

	CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC5255 PDA Lab	CO1		2					3			2		1
	CO2	1	1			1	1	2	1	2		2	2
	CO3		1			1	3	3	1	2			2
	CO4	1	1	1	1		3	2	1	2	2		2

Mapping of COs with Pos

Detailed syllabus:

Cycle 1:

1) Graph algorithms

a) Graph search algorithms
   i. Depth first search
   ii. Breadth first search

b) Spanning tree algorithm
   i. Kruskal's algorithm

c) Shortest path algorithm
   i. Dijkstra algorithm
   ii. Floyd- Warshall algorithm

d) Steiner tree algorithm

2) Computational geometry algorithm

a) Line sweep method

b) Extended line sweep method

Cycle 2:

3) Partitioning algorithms

I) Group migration algorithms

a) Kernighan –Lin algorithm

b) Extensions of Kernighan-Lin algorithm

i) Fiduccias –Mattheyses algorithm

ii) Goldberg and Burstein algorithm

II) Simulated annealing and evolution algorithms

a) Simulated annealing algorithm

b) Simulated evolution algorithm

III) Metric allocation method

4) Floor planning algorithms

i) Constraint based methods

ii) Integer programming based methods

iii) Rectangular dualization based methods

iv) Hierarchical tree based methods

v) Simulated evolution algorithms

vi) Time driven Floorplanning algorithms

5) Routing algorithms

I) Two terminal algorithms

a) Maze routing algorithms

i)Lee's algorithm

ii) Soukup's algorithm

iii) Hadlock algorithm

b) Line-Probe algorithm

c) Shortest path based algorithm

II) Multi terminal algorithm

a) Stenier tree based algorithm

i) SMST algorithm

ii) Z-RST algorithm

Reading:

1) Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic, 1998.
2) Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.