Total No. of Questions—**12**] [Total No. of Printed Pages—**4**

[4062]-154

S.E. (Electronics/E & TC) (First Semester) EXAMINATION, 2011

DIGITAL LOGIC DESIGN

(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. **:—** (*i*) Answer **3** questions from Section I and **3** questions from Section II.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data, if necessary.

SECTION I

1. (*a*) What is digital comparator ? Design two bit digital comparator and implement using logic gates. [10]

(*b*) Design four bit binary to gray code converter and implement using logic gates. [8]

Or

2. (*a*) Minimize the following equation using K-map and realize it using NAND gates only. [10]

$$Y = \Sigma M\ (0,\ 1,\ 2,\ 3,\ 5,\ 7,\ 8,\ 9,\ 11,\ 14)$$

P.T.O.

(*b*) Design and implement the following function using 8 : 1 MUX.

$$Y = \Sigma M\ (4,\ 5,\ 8,\ 9,\ 11,\ 12,\ 13,\ 15)$$ [8]

3. (*a*) Draw and explain SR flip-flop using NAND gates. [8]

(*b*) Convert D to T flip-flop and vice versa. [8]

Or

4. (*a*) Design and implement the following counter-states using JK flip-flop and avoid the lockout condition : [8]

$$0 - 2 - 4 - 6 - 7 - 0.$$

(*b*) Design MOD5 asynchronous counter, and also draw the waveforms and mention significance of glitch. [8]

5. (*a*) Write short notes on :

(*i*) Library [2]

(*ii*) Entity [2]

(*iii*) Architecture with modelling style. [4]

(*b*) Explain the difference between signal and variable used in VHDL. [8]

Or

6. (*a*) Write a VHDL code for four bit ALU using case when statement. [8]

(*b*) Write a VHDL code for JK flip-flop with asynchronous reset. [8]

SECTION II

7. (*a*) Compare Mealy and Moore sequential machine with reference to block diagram, state diagram, hardware and speed. [8]

(*b*) Design and implement 1011 sequence detector using Mealy machine. [10]

Or

8. (*a*) Design and implement digital hardware for the following Fig. (*a*) using D flip-flop and identify the sequence. [8]

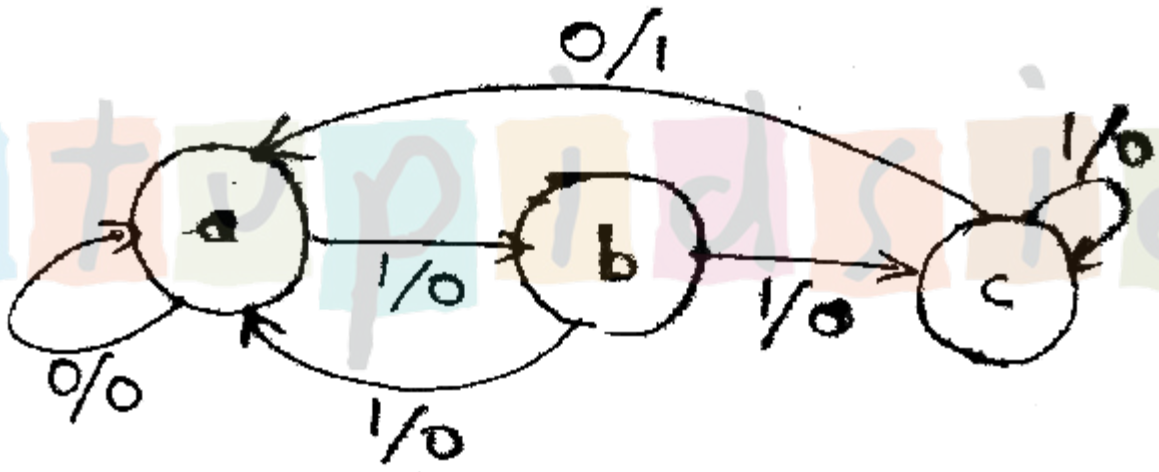

Fig. (*a*)

(*b*) Design and implement the ASM chart for a 3 bit binary counters having one enable line E such that E = 1 (Counting enabled), E = 0 (counting disabled). [10]

9. (*a*) Write a short note on classification of logic families in detail. [8]

(*b*) State the following characteristics of digital IC's (TTL). [8]

(*i*) Speed of operation

(*ii*) Fan in fan out

(*iii*) Noise Margin

(*iv*) Voltage parameter

Or

10. (*a*) Draw and explain two input totem pole output TTL NAND gate. [8]

(*b*) Draw CMOS circuit for NAND gate and NOR gate. [8]

11. (*a*) Design a combinational logic circuit using PROM, the circuit accepts three bit binary number and generates its equivalent excess 3 code. [8]

(*b*) Explain in detail the architecture of PLDs. [8]

Or

12. (*a*) Implement the function using PLA. [8]

$F_1 = \bar{A}B + A\bar{C} + \bar{A}\,B\,\bar{C}$

$F_2 = \overline{A\bar{C} + \bar{B}C}$

(*b*) Design 16K × 8 RAM using two 4K × 8 RAM ICs. [8]