Anna University Exams May/June 2014 — Regulation 2013

Rejinpaul.com Important Questions – 2nd Semester BE/B.TECH

**Important Questions (pattern) DPSD**

CS6201 Digital Principles and System Design

**All answers are available as an annexure of book "Digital Principal and System Design AU R 2013"**

1. Reduce the following equations using Karnaugh map technique :
   i. $f(ABC) = \sum m\,(0,1,3,7) + \sum d(2,5)$.
   ii. $F(w,x,y,z) = \sum m(0,7,8,9,10,12) + \sum d(2,5,13)$.

2. i. Minimize the following expression using Karnaugh map.
   $Y = A'BC'D' + A'BC'D + ABC'D' + AB'C'D + ABC'D$
   ii. State and prove the De Morgan's theorems.

3. i. Define Prime Implicant and Essential Prime Implicant.
   ii. Write the procedure for obtaining the logic diagram with NAND gates from a Boolean function.
   iii. Implement the switching function.
   $F(x,y,z) = \sum m\,(1,2,3,4,5,7)$ with NAND gates.

4. Design a combinational circuit that comprises only of NOR gates for the following expression giving the input output relation,
   $Y = ABC' + AC + B'C$.

5. Minimize the expression using Quine McCluskey (Tabulation) method.
   $y' = A'BC'D' + A'BC'D + ABC'D' + ABC'D + AB'C'D + A'B'C\,D'$

6. Design a full adder using 2 half adders.

7. Design Half and Full Subtractor circuits.

8. Design a circuit that converts 8421 BCD code to Excess-3 code.

9. (i) Design a BCD to Excess – 3 code converter using truth table and k – map simplification.
   (ii) Draw the schematic of a magnitude comparator and give its truth table.

10. Design a combinational circuit to convert binary to gray code.

11. Implement the switching function F = ∑m (0, 1, 3, 4, 12, 14, 15) using an 8 input MUX.

12. Implement a full adder with two 4 × 1 multiplexers

13. i. Design a combinational logic circuit using a suitable multiplexer to realize the following Boolean expression $Y = AD' + B'C + BC'D'$.

    ii. Compare and contrast between encoders and multiplexer.

14. i. Write short notes on the basic configuration of the three types of programmable Logic Devices.

    ii. Draw the signals of a 32 X 8 RAM with control input. Show the external connections necessary to have a 128 X 8 RAM using a decoder and replication of this RAM.

15. Implement the switching functions

    $Z_1 = a\bar{b}\bar{d}e + \bar{a}\bar{b}\bar{c}\bar{d}\bar{e} + bc + de$

    $Z_2 = \bar{a}\bar{c}e$

    $Z_3 = bc + de + \bar{c}\bar{d}\bar{e} + bd$

    $Z_4 = \bar{a}\bar{c}e + ce$ using $5 \times 8 \times 4$ PLA

16. Implement the following function using PLA

    $A(x, y, z) = \sum m\,(1, 2, 4, 6)$

    $B(x, y, z) = \sum m\,(0, 1, 6, 7)$

    $C(x, y, z) = \sum m\,(2, 6)$

17. Using D flip-flops, design a synchronous counter which counts in the sequence, 000, 001, 010, 011, 100, 101, 110, 111, 000.

18. Design a shift register using JK flipflops.

19. i. Draw a 4-bit ripple counter with D flip flops

    ii. Write the HDL for the above circuit.

20. A synchronous counter with four $JK$ flip flop has the following connections:

    $J_A = K_A = 1$,

    $J_B = Q_A Q'_D$, $\quad K_B = Q_A$

    $J_C = K_C = Q_A Q_B$

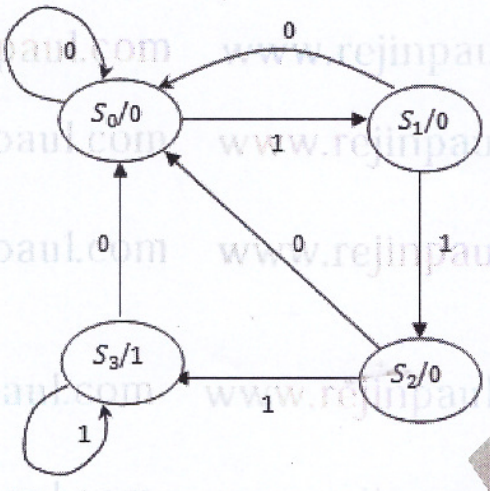
    $J_D = Q_A Q_B Q_C$ and $K_D = Q_A$

    Determine the modulus $n$ of the counter, and draw the output waveforms of the same.

21. Design a synchronous counter using JK flip flops to count the following sequence:

    "1 – 3 – 15 – 5 – 8 – 2 – 0 – 12 – 6 – 9".

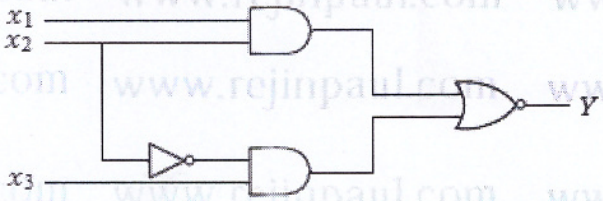
22. Design the sequential circuit specified by the state diagram using JK flip flop.




23. i. Explain the types of hazards in digital circuits.
    ii. Implement the switching function F = ∑m(1, 3, 5, 7, 8, 9, 14, 15) by a static hazard free 2 level AND-OR gate network.
24. Explain the steps for the design of asynchronous sequential circuits.
25. Design an asynchronous sequential circuit that has 2 inputs $X2$ and $X1$ and one output $Z$. When $X1 = 0$, the output $Z$ is 0. The first change in $X2$ that occurs while $X1$ is 1 will cause output $Z$ to be 1. The output $Z$ will remain 1 until $X1$ returns to 0.
26. Find a circuit that has no static hazards and implements the Boolean function
    $F(A, B, C, D) = \sum m(1, 3, 5, 7, 8, 9, 14, 15)$
27. i. Explain the working principle of switch debounce logic.
    ii. Determine whether the circuit is stable or not whose excitation function is given by $Y = (x_1y)'x_2$.
28. Derive a circuit specified by the following flow table.

| | XY 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| A | A,0 | A,0 | A,0 | B,0 |
| B | A,0 | A,0 | B,1 | B,1 |

29. Determine whether the following circuit has a static hazard or not. If yes, design a hazard free logic for the same input and output relation.




30. (i) Simplify the following Boolean function F together with don't – care condition d, and then express the simplified function in sum of minterms.

$F(w, x, y, z) = \sum(1, 3, 7, 11, 15) + \sum d(0, 2, 5)$

(ii) Implement the following Boolean function with NAND gates.

$F(x, y, z) = (1, 2, 3, 4, 5, 7)$

**For all previous year QUESTIONS WITH ANSWERS (from 2009 onwards) refer the annexure of the book. ALL THE BEST**