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## 1) Special software to create a job queue is called

- a) driver
- b) spooler
- c) interpreter
- d) linkage editer
- 2) When a process is rolled back as a result of deadlock the difficulty arises is
- a) Starvation
- b) System throughput
- c) low device utilization
- d) cycle stealing
- 3)On recieving an interrupt from an I/O device the CPU
- a) Halts for a predefined time.
- b) Branches off the interrupt service routine after completion off the current instruction.
- c) Branches off to the interrupt service routine immediately.
- d) hands over the control of address bus and data bus to the interrupting service.
- 4) Which of the following is true of the auto increment addressing mode?
- 1. It is useful in creating sef relocating code.
- 2)If it is induced in an instruction set architecture, than an additional ALU is required for effective address calculation.
- 3) The amount of increment depends on the size of the data item accessed.
- a) 1 only.
- b)2 only
- c) 3 only
- d) 2 and 3 only
- 5) The primary purpose of an operating system is
- a) To make the most efficient use of the computer hardware.
- b) to allow people to use the computer.
- c) To make the system programmers employed.
- d) to make computers easy to use.

6)consider the cpu intensive processes which require 10,20,30 time units and arrive at time 0,2,6 respectively.how many context switches are needed if the operating system impements a shortest remaining time first sceduling algorithm? Do not count the context switches at the time 0 and end.

- a) 1
- b) 2
- c) 3
- d) 4
- 7) consider a system having n resources of the same type. These resources are shared by 3 processes A,B,C .These have peak demands of 3,4,6 respectively. For what value of n deadlock won't occour.
- a) 15
- b) 9
- c) 10
- d) 13

In which addressing mode the effective address of the operand is

- > CDS UPSC
- > CEEB
- > CEED
- > CG PET
- > CG PET
- > CG PMT
- > Chemistry
- Entrance
- → CLAT
- → CMAT > CMS UPSC
- → COMEDK
- > COMEDK UGET
- > CPF UPSC
- > CSAT
- > CSIF UPSC
- > CTET
- > CUCET
- > Data Entry
- Operator
- > Delhi
- Metro(DMRC) > Delhi TET
- > DRDO
- > DSSSB
- > DU B.Ed
- Entrance
- > DUBFIEd
- Entrance
- > DU CATE > DU LLM-LLB
- > DUMET
- > EAMCET Engineering
- > EAMCET
- Medicine
- > ECIL > EIL
- > el itmus
- > FSIC
- > FCI
- > FMS > FTII
- → GATE
- > GBTU SEE
- > GPAT
- > GPAT
- › Gujarat TET
- > GUJCET
- > HAL
- > Haryana B.Ed.
- > Haryana TET > Haryana TET
- > HM Entrance
- > HP CPMT
- > HP TET
- > HPCL
- > HPPSC
- > HSST
- > IBPS 2012
- > ICET
- > ICMR > ICSE
- > IES
- > IFS
- > Ignou-b-ed
- Entrance
- > IIFT MAL TIL <
- > IIT JEE

computed by adding a constant value to the content of the register? > Indian Oil -**ICOL** a) absolute mode. > IPU B.Ed b) indirect mode **Entrance** c) immediate mode > IPU CET d) index mode > IRDA > ISAT 9)the process of organizing the memory into two banks to allow 16 bit > ISC and 8 bit data operation is called > ISRO a) bank switching > JCECE Medical Entrance b) indexed mapping → JEST c) two way memory interleaving > JIPMER d) memory segmentation ) JKCET Paper > JMI B.Ed 10)a one dimensional array A has indices 1-75. Each element is a string > JMI engineering and takes up three memory words. The array is stored in location 1120 entrance decimal. The starting address of A[49] is > JMI M.Ed a) 1267 Entrance b) 1164 > JNU MCA c) 1264 Entrance > Karnataka Cet d) 1169 > Karnataka TET > Kerala B Fd 11) The microsystems stored in the control memory of a processor have **Entrance** a width of 26 bits. Each microinstruction is divided into three fields: a > Kerala CET microoperation field of 13 bits, a next address field(X), and a MUX select KEAM field(Y). There are 8 status bits in the inputs of the MUX. How many bits > Kerala CET **KEAM** are there in the X and Y fields and what is the size of the control > Kerala PSC memory in number of words? > Kerala TET a) 10,3,1024 > KMAT-MBA MCA b) 8,5,256 > KPSC c) 5,8,2048 > KVS PGT d) 10,3,512 > Law Entrance > LIC AAO 12) The use of multiple register windows with overlap causes a reduction > LIC AAO in the number of memory accesses for > LIC FSE 1.function locals and parameters > M.Ed Entrance register saves and restores. > M.Sc. Biotechnology 3. instruction fetches. > Manipal PMT a) 1 only > MAT b) 2 only > MBA Entrance c) 3 only > MCA Entrance d) 1,2,and 3 > MCFT > Medical 13) Which of the following about relative addressing mode is false? Entrance a) it enables reduced instruction size. > Mh Arch Entrance b) it allows indexing of array element with same instruction. > MH B.Ed c) it enablles easy relocation of data. Entrance d) it enables faster address calculation than absulute addressing. > MH CET > MHT AAC CET 14) Substitution of values for names (whose values are constants) is > MP DMAT done in ' > MP MET a) local optimization > MP PET b) loop optimization > MP Pre B.Ed c) constant folding **Entrance** > MPPSC d) strength reduction > NAT 15)A root a of eq f(x)=0 can be computed to any degree of accuracy if a > NATA > NCHMCT JEE good initial approximation x0 > NDA is chosen for which > NIFT a) f(x0)>0> NIMCET b) f(x0)f''(x0)>0> NTPC c) f(x0)f''(x0)<0> ONGC

16) consider the polynomial p(x)=a0+a1x+a2x\*x+a3x\*x\*x. The mininum

OPSCOrissa JEE

d) f''(x0)>0