$A_v = -\frac{R_c \| r_o}{r_e}$

$= 36$

$Z_o = R_c \| r_o$

$Z_i = R_c$

$A(1+\beta A) =$

$100(1+\beta(100)) = \frac{9}{10}$

IWL

3rd Semester B.Tech Examination, Nov. 2004

ANALOGUE ELECTRONICS CIRCUITS

Full Marks : 70

Time : 3 hours

Group—A is compulsory and answer any five questions from Group—B

The figures in the right-hand margin indicate marks

Symbols used throughout carry usual meaning

State assumptions clearly in choosing any component value or data if not specified

GROUP—A

1. Answer the following: 2 × 10

(*a*) State Barkhausen criterion, i.e., the condition necessary to sustain sinusoidal oscillation.

(*b*) What is the concept of virtual ground?

(*c*) Define the safe operating area of a transistor with suitable sketches.

(*Turn Over*)

(*d*) Draw the electrical model of a piezo-electric crystal.

(*e*) State three advantages of class B power amplifier over class A.

(*f*) Explain the origin of crossover distortion? How can this be minimized?

(*g*) How do coupling and bypass capacitors affect frequency response of an amplifier stage?

(*h*) What kind of circuit is used in the output stage of an OPAMP and why?

(*i*) Mention typical bandwidth for an audio amplifier, TV set, for an 80 column monitor and an oscilloscope amplifier.

(*j*) Adding a pre-amplifier to an audio amplifier increases the voltage gain by 60 dB. What is the corresponding factor by which the voltage is increased?

GROUP—B

2. For the network of *Fig. 1*

(*a*) Determine r_e

(*b*) Calculate Z_i and Z_o

(*c*) Find A_v and A_i

(*d*) Repeat parts (*b*) and (*c*) above with $r_o = 25\ k\Omega$.

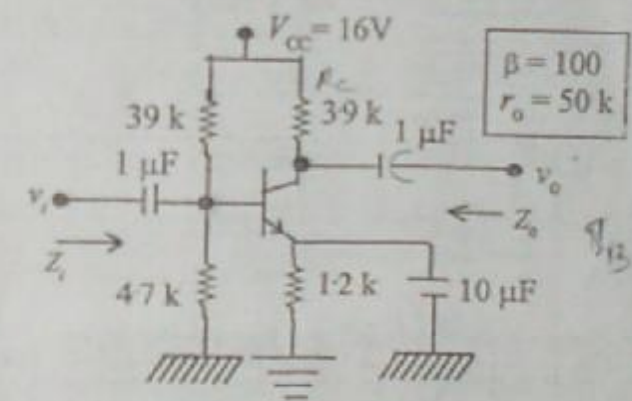

Fig. 1

3. (*a*) For the circuit in *Fig. 2*, the parameters are: $V^+ = 10\,V$ and $V^- = -10V$, $R_S = 0$, $R_E = 5\,k\Omega$. The transistor parameters are $V_{BE}(on) = 0{\cdot}7\,V$ and $V_A = \infty$ and the transistor current gain β is in the range of $75 \leq \beta \leq 125$. (*i*) Determine the value of C_E such that the low-frequency 3 dB point is $f_B \leq 200\,Hz$, (*ii*) From the results of part (*i*), determine the range in frequencies f_B and f_A.

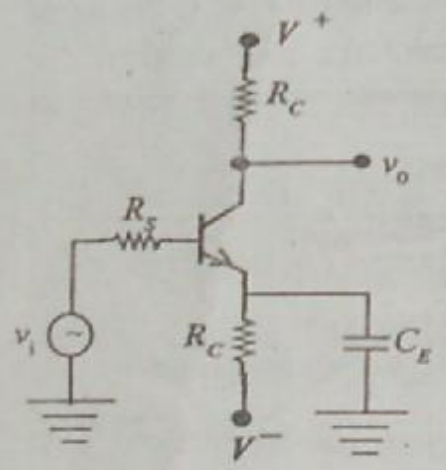

Fig. 2

(*b*) For the circuit in *Fig. 3* the transistor parameters are: $K_n = 0{\cdot}5\ \text{mA}/V^2$, $V_{TN} = 2\text{V}$ and $\lambda = 0$. Determine the maximum value C_L such that the bandwidth is at least BW = 5 MHz. State any approximations or assumptions that you make. What is the magnitude of the small–signal midband voltage gain? 5+5

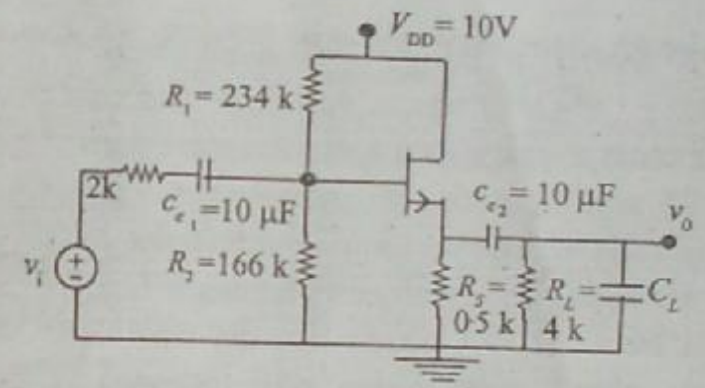

Fig. 3

4. (*a*) For the OPAMP in the voltage follower circuit in *Fig. 4*, the open loop gain is 10^4, $R_I = 100\,\text{k}\Omega$, and $R_0 = 200\,\Omega$. Determine the closed loop voltage gain, R_{of} and R_{if}.

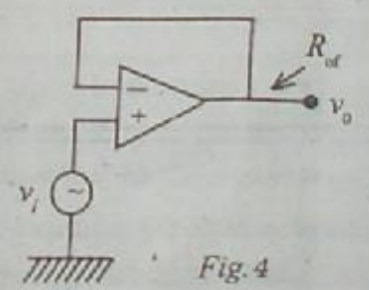

Fig. 4

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(*b*) It is desired to design a summing circuit (using OPAMP) whose output in volts is the class average on a quiz. The class size is 25 and all grades are integers between one and ten. The maximum output voltage is 10 V and the minimum resistance that can be used is 1 kΩ. Design the circuit. Now check your design with following grade distribution.

Number of students :	0	1	0	2	1	4	7	4	3	3
Quiz Grade :	1	2	3	4	5	6	7	8	9	10

(*c*) Sketch the phase-shift oscillator using (*i*) an OPAMP, (*ii*) a JFET. At what frequency will the circuit oscillate? 2+4+4

5. (*a*) Sketch the topology of a generalized resonant circuit oscillator, using impedances Z_1, Z_2, Z_3. Reduce this circuit to Hartley and Colpitts oscillator choosing components suitably? At what frequency will these circuits oscillate?

(*b*) Derive an expression for v_0 in terms of input signals and the four resistors for the instrumentation amplifier shown in *Fig. 5*.

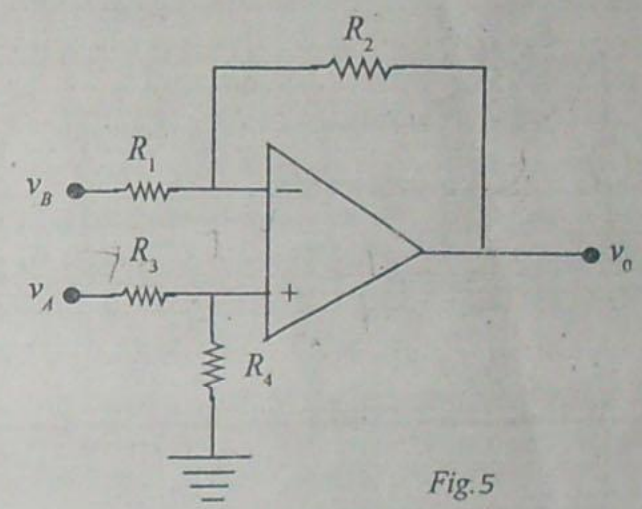

Fig. 5

(*c*) If the above circuit is to be used as subtractor, for $R_1 = R_3 = 10\,k$ ~~find $R_2 = R_4$~~ so that $v_0 = 2v_A - 3v_B$. $4+2\frac{1}{2}+2\frac{1}{2}+1$

6. The JFET in the amplifier circuit of *Fig. 6* has $V_p = -4$ V and Idss = 12 mA, and at $I_D = 12$ mA the output resistance $r_0 = 25$ k. 10

(*a*) Determine the dc bias quantities V_g, I_D, V_{gs} and V_D.

(*b*) Determine the values of g_m and r_0.

(*c*) Replace the JFET with its small signal model, thus obtaining the small-signal equivalent circuit of the amplifier.

(*d*) Use the equivalent circuit in (*c*) to determine R_{in} and v_g / v_{in}.

(*e*) Use the equivalent circuit to determine v_0 / v_g.

(*f*) Find the overall gain v_0 / v_{in}.

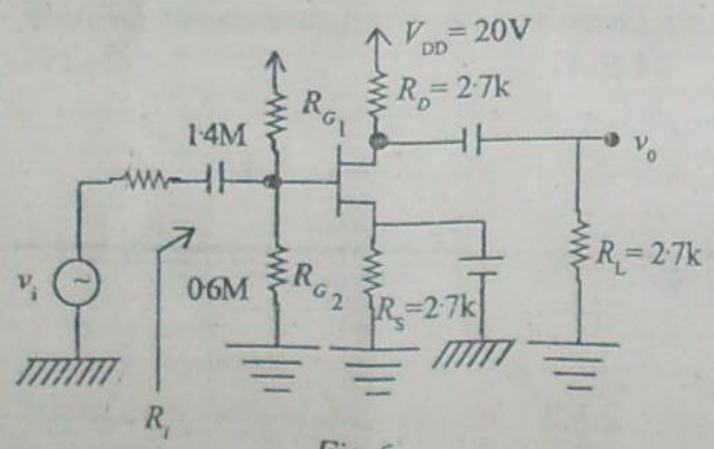

Fig. 6

7. (*a*) For the class-A amplifier shown in *Fig. 7*, show that the maximum theoretical conversion efficiency for a symmetrical square wave input is 50 per cent.

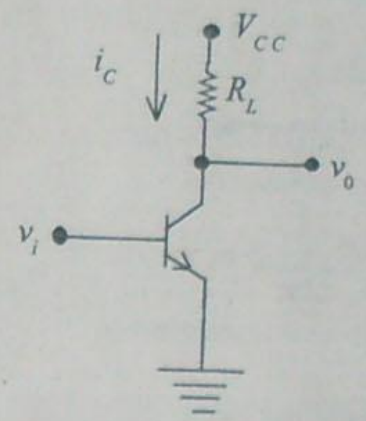

Fig. 7

(*b*) Design the idealized class-B output stage, as shown in *Fig. 8*, to deliver an average of 25 W to an 8 ohm speaker. The peak output voltage must be no larger than 80 per cent of supply voltage V_{CC}. Determine

(*i*) The required value of V_{CC}

(*ii*) The peak current in each transistor

(*iii*) The average power dissipated in each transistor

(*iv*) The power conversion efficiency.

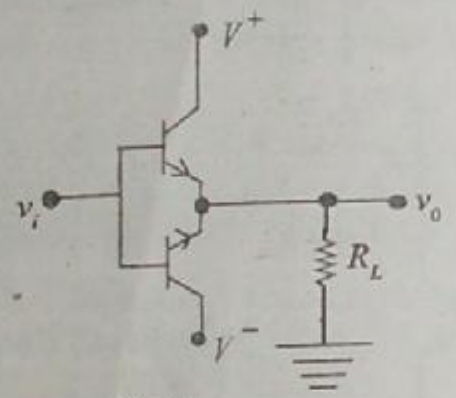

Fig. 8

(*c*) Define the safe operating area of a transistor with suitable sketches, graphs etc. $2\frac{1}{2} + 5 + 2\frac{1}{2}$

8. (*a*) Consider a general feedback system with parameters $A = 10^6$ and $A_f = 100$. If the magnitude of A decreases by 20 per cent, what is the corresponding per cent change in A_f.

(*b*) Draw the schematic of a series-shunt feedback topology. Derive expressions for closed loop voltage gain, input resistance and output resistance after feedback.

(*c*) A series-shunt feedback amplifier represented by *Fig. 9* and using an basic voltage amplifier operates with $V_S = 100$ mV, $V_f = 90$ mV and $V_0 = 10$ V. What are the values of A and β.

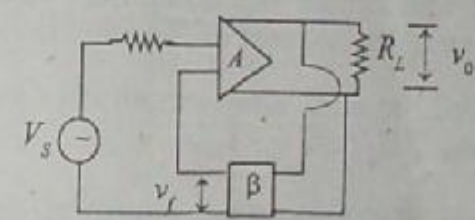

Fig. 9

(*d*) Draw the pin configuration for OPAMP LF-411. 2+2+4+2