

Registration No. :

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Total number of printed pages – 3

B. Tech
PCEC 4202

Fourth Semester Examination – 2013

DIGITAL ELECTRONICS CIRCUITS

BRANCH : AEIE / BIOMED / CSE / EEE / ELECT / EC / ETC / IT / IEE / EIE

QUESTION CODE : A 341

Full Marks – 70

Time : 3 Hours

Answer Question No. 1 which is compulsory and any five from the rest.

The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2×10
- (a) What do you mean by 'digits' and 'base' of the Boolean number ? Under what condition an end carry will occur during 1' complement method of subtraction ?
- (b) Under what condition the output of an two input EX-OR gate remain always at logic ZERO level ? Justify with logical expression/diagram.
- (c) Add the following addition and convert the results in decimal system ? R is the base of the number.
- $(31)_R + (39)_R$
- (d) Realize a combinational circuit which produces output 1 when there is even number of ones in the input.
- (e) What is 'Fan in' and 'Fan out' of the integrated logic circuits ?
- (f) What is a Flip-flop ? How many D Flip-flops are required to design MOD-3 counter ?

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- (g) How many $32\text{ K} \times 1$ RAMs are required to obtain a memory with word capacity of 128 K ? The word length is of eight bits.
- (h) What is Race problem in sequential circuits? How it is avoided?
- (i) State two basic differences between synchronous and asynchronous sequential circuit?
- (j) Draw the state diagram of a decade counter.
2. (a) (i) Prove that sum of all miniterms of a Boolean function of n variable is one. 2.5
- (ii) Show that the dual of EX-OR is equal to its complement. 2.5
- (b) Establish the following identities of Boolean algebra: 2.5×2
- (i) $A + AB = A$
- (ii) $(A + B)(A + C) = A + BC$
3. (a) A majority logic function is a Boolean function that is equal to 1 if the majority of variables are equal to 1, equal to 0 otherwise. Design a combinational circuit for four bit majority function. 5
- (b) Write characteristics equation and table for a full adder circuit. Then, implement the full adder with decoder and NAND gates. 5
4. (a) Simplify the following function using K-Map:
- $$F(A, B, C, D) = \sum m(1, 4, 5, 6, 7, 13).$$
- And then, write the simplified functions in POS and SOP form. 5
- (b) A PN flip flop has four operation, no change, clear to 0, set 1, and complement, when inputs P and N are 00, 01, 10, and 11 respectively. Write excitation table, characteristics equation of the PN flip flop and realize the flip flop using logic gates. 5

5. (a) A sequential circuit has two flip flop A and B and one output x. The circuit is described by the following input equation : 7
- $$J_A = x, \quad J_B = x$$
- $$K_A = B', \quad K_B = A$$
- (i) Derive the state equation $A(t+1)$ and $B(t+1)$ by substituting the input equation for the J and K variable.
- (ii) Draw the state table and state diagram of the circuit.
- (b) What is edge triggering ? Explain how race problem can be avoided using edge triggering ? How it 3
6. (a) Design a counter which will count the following repeated binary sequence: 0, 2, 5, 6, 7, 0, 2....., using T flip-flop 5
- (b) What is a shift register ? Explain the principle of a 4-bit Serial-in parallel-out shift register. 5
7. (a) Explain briefly basic configuration of programmable logic devices (PLDs). 5
- (b) Draw a PLA circuit to implement the function 5
- $$F1 = A'B + AC' + ABC$$
- $$F2 = (AB + AC + BC)'$$
8. Write short notes on any **two** : 5×2
- (a) Encoders
- (b) C-MOS invertors
- (c) HDL
- (d) Carry look ahead adder.