

## **EC 2404 - ELECTRONIC SYSTEM DESIGN LAB**

1. REGULATION CHARACTERISTICS OF BUCK –BOOST CONVERTER
2. REGULATION CHARACTERISTICS OF FLYBACK CONVERTER
- 3 (i) DESIGN OF AM TRANSCEIVER
- 3 (ii) DESIGN OF FM TRANSCEIVER
4. DESIGN OF WIRELESS DATA MODEM.
5. PCB LAYOUT DESIGN USING CAD
6. DESIGN OF DC VOLTAGE REGULATOR USING SCR
7. MICROCONTROLLER BASED SYSTEM DESIGN.
8. DESIGN OF PROCESS CONTROL TIMER
9. DESIGN OF INSTRUMENTATION AMPLIFIER
10. DSP BASED DIGITAL FUNCTION GENERATOR
11. SIMULATION OF DC VOLTAGE REGULATOR USING SCR
12. SIMULATION OF AC VOLTAGE CONTROLLER USING SCR

## **REGULATION CHARACTERISTICS OF BUCK-BOOST CONVERTER**

**EXPT NO: 1**

**AIM:**

To determine the closed loop response of the Buck-Boost converter and plot the regulation characteristics.

**APPARATUS REQUIRED:**

1. VSMPS-07A Trainer
2. Pulse patch chords
3. (0-30V) DC supply
4. CRO

**FORMULA:**

Output voltage  $V_0 = (-D / 1-D) V_s$  Volts

Where  $V_0$  = Converter Output Voltage, Volts

$V_s$  = Converter input voltage, volts

$D$  = Duty Cycle ( $t_{on} / T$ )

**THEORY:**

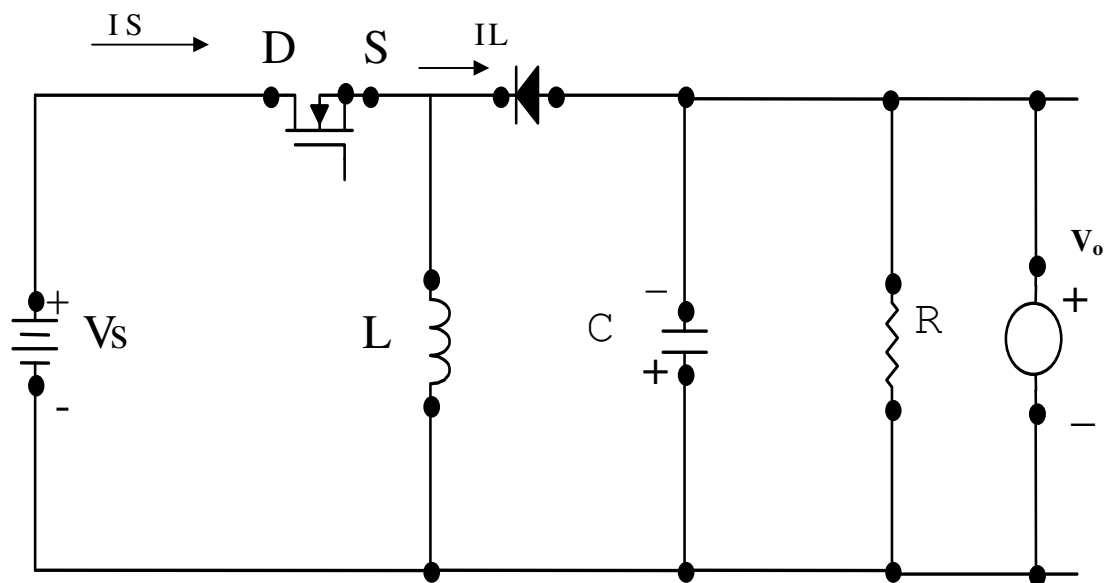
The Buck Boost is a popular non-isolated, inverting power stage topology, sometimes called a step up/down power stage. The Buck boost power stage is chosen because the output voltage is inverted from the input voltage and the output voltage can be either higher or lower than the input voltage. However the output voltage is opposite in polarity from the input voltage. The Buck Boost converter circuit consist of MOSFET switch Q, inductor L, diode D, filter capacitor C and load resistor R.

**CONNECTION PROCEDURE:**

- Connect P8 of PWM generator to PWM input of Buck-Boost converter circuit.
- Connect P4 of Buck-Boost converter circuit to P7 of PWM generator.
- Set switch SW1 to downward direction to select the closed loop operation.

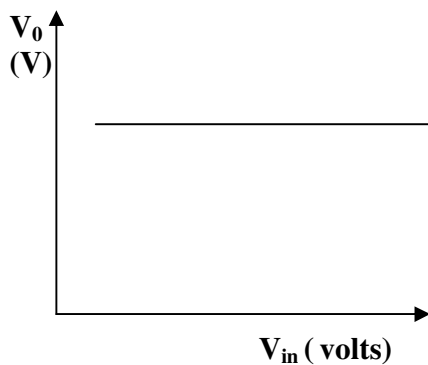
- Connect (0-30V) DC regulated power supply across P1 and P2 terminals of the trainer module and set the voltage at 15 V.

**CIRCUIT DIAGRAM:**

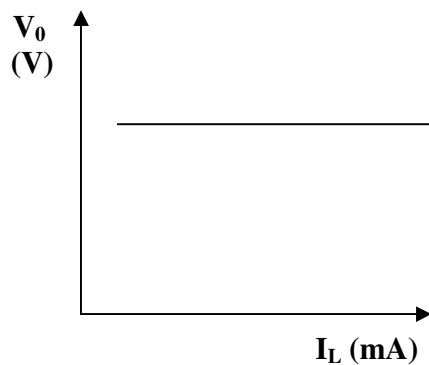


**Buck -Boost Converter**

Model Graph :



**Line Regulation**



**Load Regulation**

## **EXPERIMENTAL PROCEDURE:**

### **A) Line Regulation:**

- Switch ON the AC power supply and the power ON/OFF switch of the trainer kit.
- View the carrier signal in CRO at T3.
- Set the switch SW1 in downward direction.
- Set the switch SW2 in downward direction.
- View the PWM signal in CRO at T1.
- Vary the Set voltage adjust POT from minimum to maximum and note down the  $t_{on}$  and T values.
- Set the PWM signal at desired duty cycle ratio (maximum 50%).
- Switch ON the variable DC supply.
- Vary the input voltage from (0-15) V and note down the corresponding output voltage across P5 and P6.
- For each input voltage value tabulate the measured output voltage values.

Set the switch SW2 in upward direction and repeat the same procedure for Buck converter.

**TABULATION (BUCK MODE):**

**A) Line Regulation:**

S.No	Input Voltage (Volts)	Output Voltage (Volts)

**B) Load Regulation:**

S.No	Load Resistor ( $\Omega$ )	Load Current (mA)	Output Voltage (Volts)

**TABULATION (BOOST MODE):**

**A) Line Regulation:**

S.No	Input Voltage (Volts)	Output Voltage (Volts)

**B) Load Regulation:**

S.No	Load Resistor ( $\Omega$ )	Load Current (mA)	Output Voltage (Volts)

**b) Load Regulation:**

- Switch ON the AC power supply and the power ON/OFF switch of the trainer kit.
- View the carrier signal in CRO at T3.
- Set the switch SW1 in downward direction.
- Set the switch SW2 in downward direction.
- View the PWM signal in CRO at T1.
- Vary the Set voltage adjust POT from minimum to maximum and note down the  $t_{on}$  and T values.
- Set the PWM signal at desired duty cycle ratio (maximum 50%).
- Switch ON the variable DC supply.
- Set the input to a constant value and vary the load resistor value, note down the corresponding output voltage across P5 and P6 output terminals of trainer module..
- For each load resistor value tabulate the measured output voltage values.
- Set the switch SW2 in upward direction and repeat the same procedure for Buck converter.

**RESULT:**

Thus the closed loop response for Boost/Buck operation of Buck-Boost converter of Line/Load regulation was determined.

1. The output voltage is maintained at ----- V with the input voltage from ----- V to ----- V for boost mode of operation.
2. The output voltage is maintained at ----- V with the input voltage from ----- V to ----- V for buck mode of operation.

## **REGULATION CHARACTERISTICS OF FLYBACK CONVERTER**

**EXPT NO: 2**

**AIM:**

To determine the closed loop response of the Flyback converter and plot the regulation characteristics.

**APPARATUS REQUIRED:**

5. VSMPS-09A Trainer
6. Pulse patch chords
7. (0-30V) DC supply
8. CRO

**FORMULA:**

Output voltage  $V_0 = (D / 1-D)(N_2/N_1) V_s$  Volts

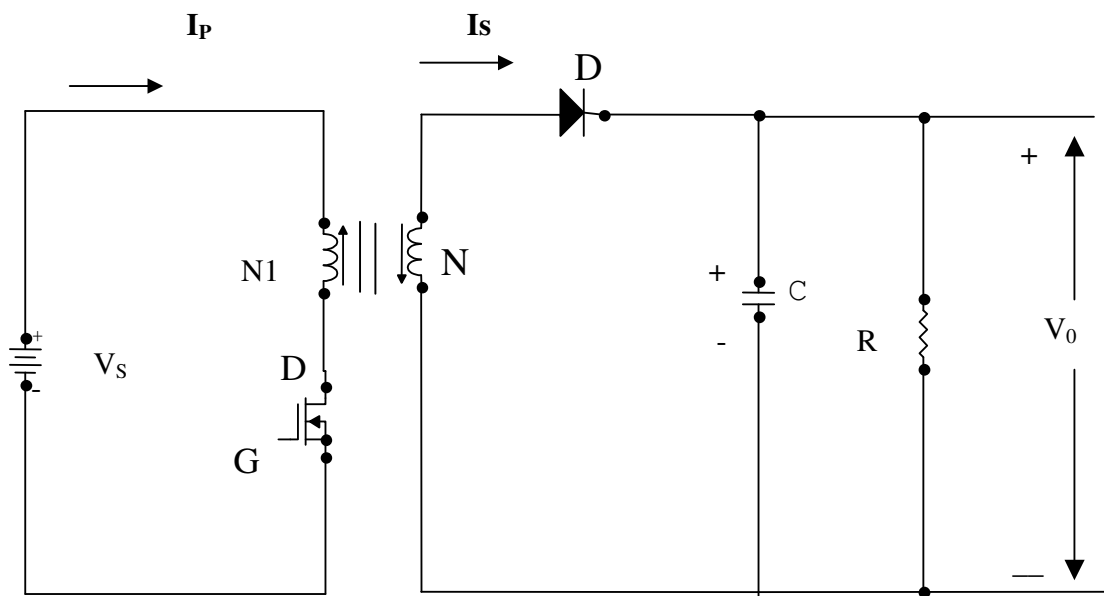
Where  $V_0$  = Converter Output Voltage, Volts  
 $V_s$  = Converter input voltage, volts  
 $D$  = Duty Cycle ( $t_{ON} / T$ )  
 $N_2 / N_1$  = Transformer turns ratio.

**THEORY :**

The flyback converter is a negative output step-up converter (i.e) it is an isolated version of the buck-boost converter. The inductor of buck-boost converter has been replaced by a flyback transformer. The input dc source  $V_s$  and switch Q are connected in series with the transformer primary. The diode D and the RC output circuit are connected in series with the secondary of flyback transformer. The circuit diagram of flyback converter is shown below.

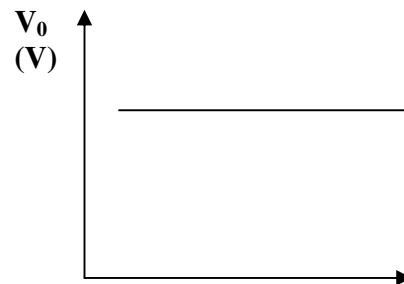
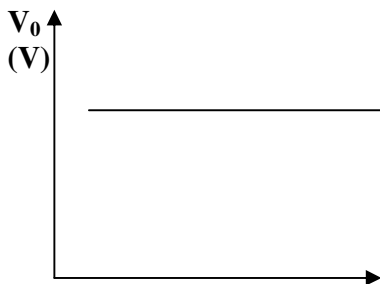


**CIRCUIT DIAGRAM :**



**FLY BACK CONVERTER**

**MODEL GRAPH:**



$V_{in}(V)$

$I_L(mA)$

**Line Regulation**

**Load Regulation**

**CONNECTION PROCEDURE :**

1. Connect P8 of PWM generator to PWM input of Flyback converter circuit.
2. Connect P4 of Flyback converter circuit to P7 of PWM generator.
3. Set switch SW1 to downward direction to select the closed loop operation.
4. Connect (0-30V) DC regulated power supply across P1 and P2 terminals of the trainer module and set the voltage at 30 V.

**TABULATION:**

**A) Line Regulation:**

S.No	Input Voltage (Volts)	Output Voltage (Volts)

**B) Load Regulation:**

S.No	Load Resistor ( $\Omega$ )	Load Current (mA)	Output Voltage (Volts)

**EXPERIMENTAL PROCEDURE:**

**A) Line Regulation:**

1. Switch ON the AC power supply and the power ON/OFF switch of the trainer kit.
2. View the carrier signal in CRO at T3.
3. Set the switch SW1 in downward direction.
4. View the PWM signal in CRO at T1.
5. Vary the Set voltage adjust POT from minimum to maximum and note down the  $t_{on}$  and T values.
6. Set the PWM signal at desired duty cycle ratio (maximum 50%).
7. Switch ON the variable DC supply.
8. Vary the input voltage from (0-30) V and note down the corresponding output voltage across P5 and P6 output terminals of trainer module.
9. For each input voltage value tabulate the measured output voltage values.

**b) Load Regulation:**

1. Switch ON the AC power supply and the power ON/OFF switch of the trainer kit.
2. View the carrier signal in CRO at T3.
3. Set the switch SW1 in downward direction.
4. View the PWM signal in CRO at T1.
5. Vary the Set voltage adjust POT from minimum to maximum and note down the  $t_{on}$  and T values.
6. Set the PWM signal at desired duty cycle ratio (maximum 50%).
7. Switch ON the variable DC supply.
8. Set the input to a constant value and vary the load resistor value, note down the corresponding output voltage across P5 and P6 output terminals of trainer module..
9. For each load resistor value tabulate the measured output voltage values.

**RESULT:**

Thus the closed loop response of flyback converter of Line/Load regulation was determined.

1. The output voltage is maintained at ----- V with the input voltage from ----- V to ----- V.

## **DESIGN OF AM TRANSCEIVER**

**EXPT NO: 3(i)**

**AIM:**

To transmit a modulating signal after amplitude modulation using VCT-08 and receive the signal back after demodulating using VCT-09.

**APPARATUS REQUIRED:**

1. VCT-08 trainer kit
2. VCT-09 trainer kit
3. CRO
4. Patch cards

**THEORY:**

**AMPLITUDE MODULATION:**

Amplitude Modulation is a process by which amplitude of the carrier signal is varied in accordance with the instantaneous value of the modulating signal, but frequency and phase of carrier wave remains constant.

The modulating and carrier signal are given by

$$V_m(t) = V_m \sin\omega_m t$$

$$V_C(t) = V_C \sin\omega_C t$$

The modulation index is given by,  $m_a = V_m / V_C$ .

$$V_m = V_{\max} - V_{\min} \text{ and } V_C = V_{\max} + V_{\min}$$

The amplitude of the modulated signal is given by,

$$V_{AM}(t) = V_C (1 + m_a \sin\omega_m t) \sin\omega_C t$$

Where

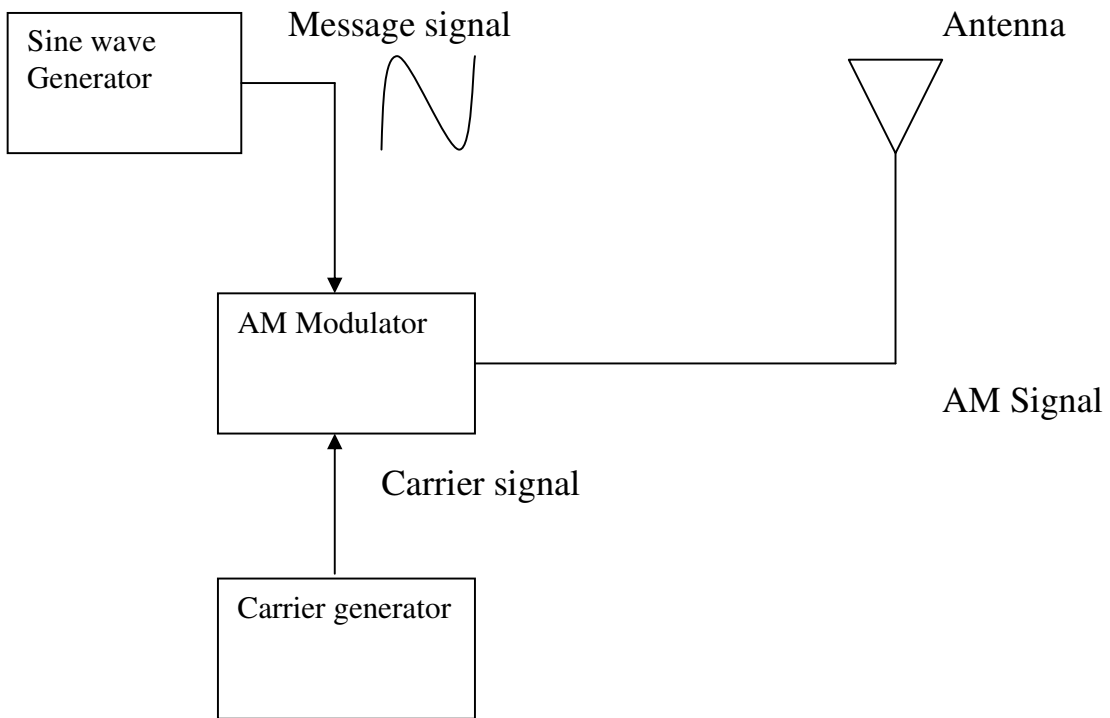
$V_m$  = maximum amplitude of modulating signal

$V_C$  = maximum amplitude of carrier signal

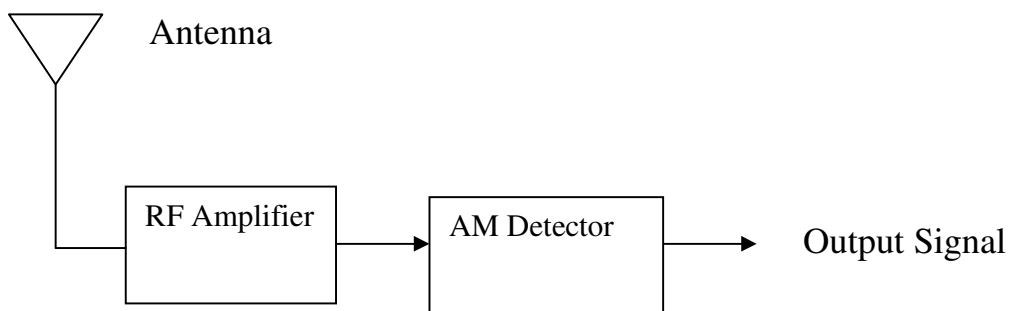
$V_{\max}$  = maximum variation of AM signal

$V_{\min}$  = minimum variation of AM signal

### AM TRANSMITTER



### AM RECEIVER



**TABULATION:**

Waveform	Amplitude (V)	Time Period (msec)	Frequency (KHz)
Modulating Signal			
Demodulated signal			

**PROCEDURE:**

1. The circuit wiring is done as shown in diagram
2. A modulating signal input given to the Amplitude modulator can also be given from a external function generator or an AFO
3. If an external signal source with every low voltage level is used then this signal can be amplified using the audio amplifier before connecting to the input of the AM modulator
4. Now increase the amplitude of the modulated signal to the required level.
5. The amplitude and the time duration of the modulating signal are observed using CRO.
6. Finally the amplitude modulated output is observed from the output of amplitude modulator stage and the amplitude and time duration of the AM wave are noted down.
7. Calculate the modulation index by using the formula and verify them.
8. The final demodulated signal is viewed using an CRO at the output of audio power amplifier stage. Also the amplitude and time duration of the demodulated wave are noted down.

**RESULT:**

The modulating signal is transmitted after amplitude modulation using VCT-08 and the signal is received back after demodulation using VCT-09



## **DESIGN OF FM TRANSCEIVER**

**EXPT : 3(ii)**

**AIM:**

To transmit a modulating signal after frequency modulation using VCT-12 and receive the signal back after demodulating using VCT-13

**APPARATUS REQUIRED:**

5. VCT-12 trainer kit
6. VCT-13 trainer kit
7. CRO
8. Patch cards

**HARDWARE DESCRIPTION OF FM TRANSMITTER TRAINER VCT-12:**

The FM transmitter trainer kit VCT-12 has the following section:

1. On-board sine wave generator
2. MIC pre amplifier with a socket for external dynamic MIC
3. Audio amplifier for amplification of low level external input signal
4. Frequency modulation
5. Telescopic whip antenna

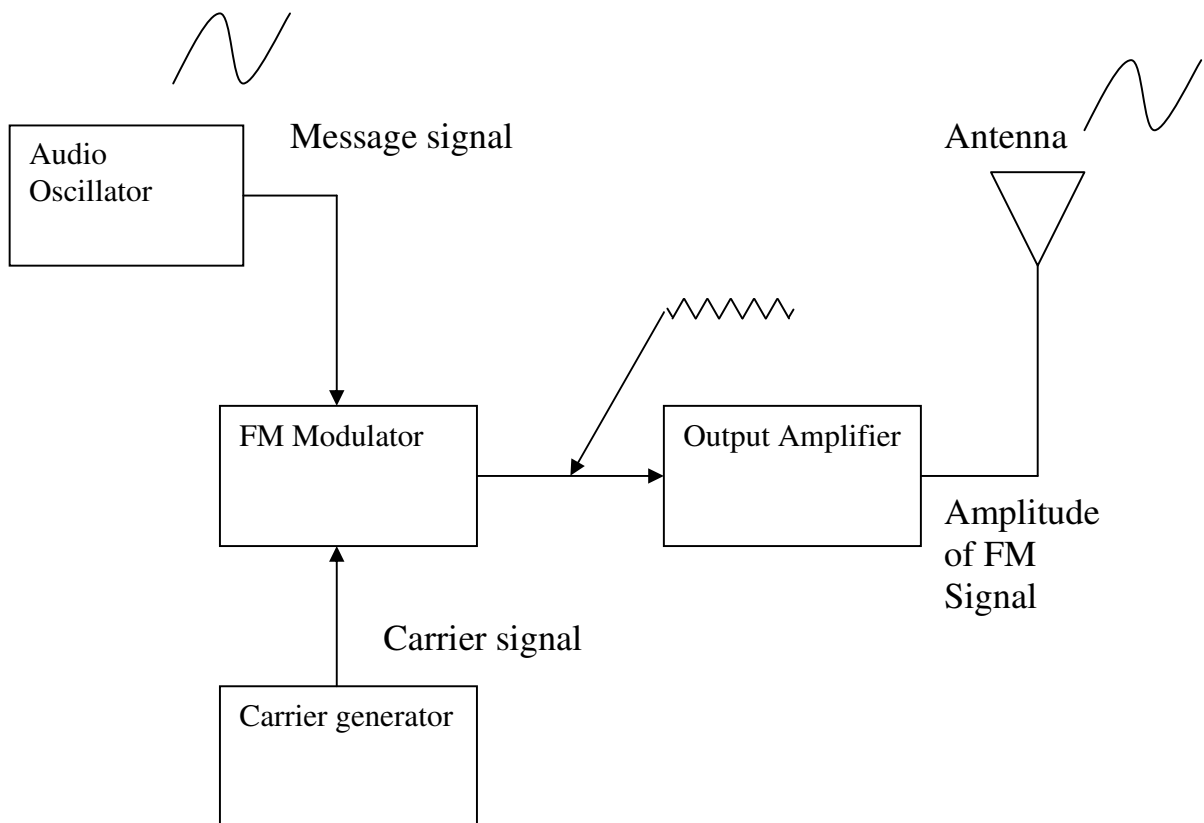
**SINE WAVE GENERATOR:**

A sine wave generator acts as an on board modulating signal source and generates an audio frequency sine wave. The amplitude of this sine wave generator varies from 0-5 V. However the output voltage from this source is controlled using a Trim pot to get an output signal in the range of 0-3V. The frequency of the signal varies from 300Hz to 15KHz. Since the amplitude of the source is large enough to modulate the carrier it need not be amplified, instead it can be directly connected to the input of the amplitude modulator.

**MIC PRE AMPLIFIER:**

The MIC pre amplifier is capable of accurately amplifying even a very low level signal, picked up by the MIC to the required level to modulate the carrier. This section has a EP socket at its input stage where, in an external dynamic MIC can be plugged in the gain of the stage can be controlled by the user by adjusting the potentiometer Pot4. The maximum gain of this stage can be achieved in this is 200. The maximum level of the input signal to this amplifier, so as to produce an amplified output without saturation is 60mV.

### FM TRANSMITTER



### **AUDIO AMPLIFIER:**

The audio amplifier stage has a BJT common emitter configuration. This audio amplifier can be used to amplify any lower level external modulating signal whose voltage level is below 100mV. The gain of this stage can also be controlled by the user by varying the pot meter POT-5. The maximum gain of this audio amplifier is 10.

### **FREQUENCY MODULATION:**

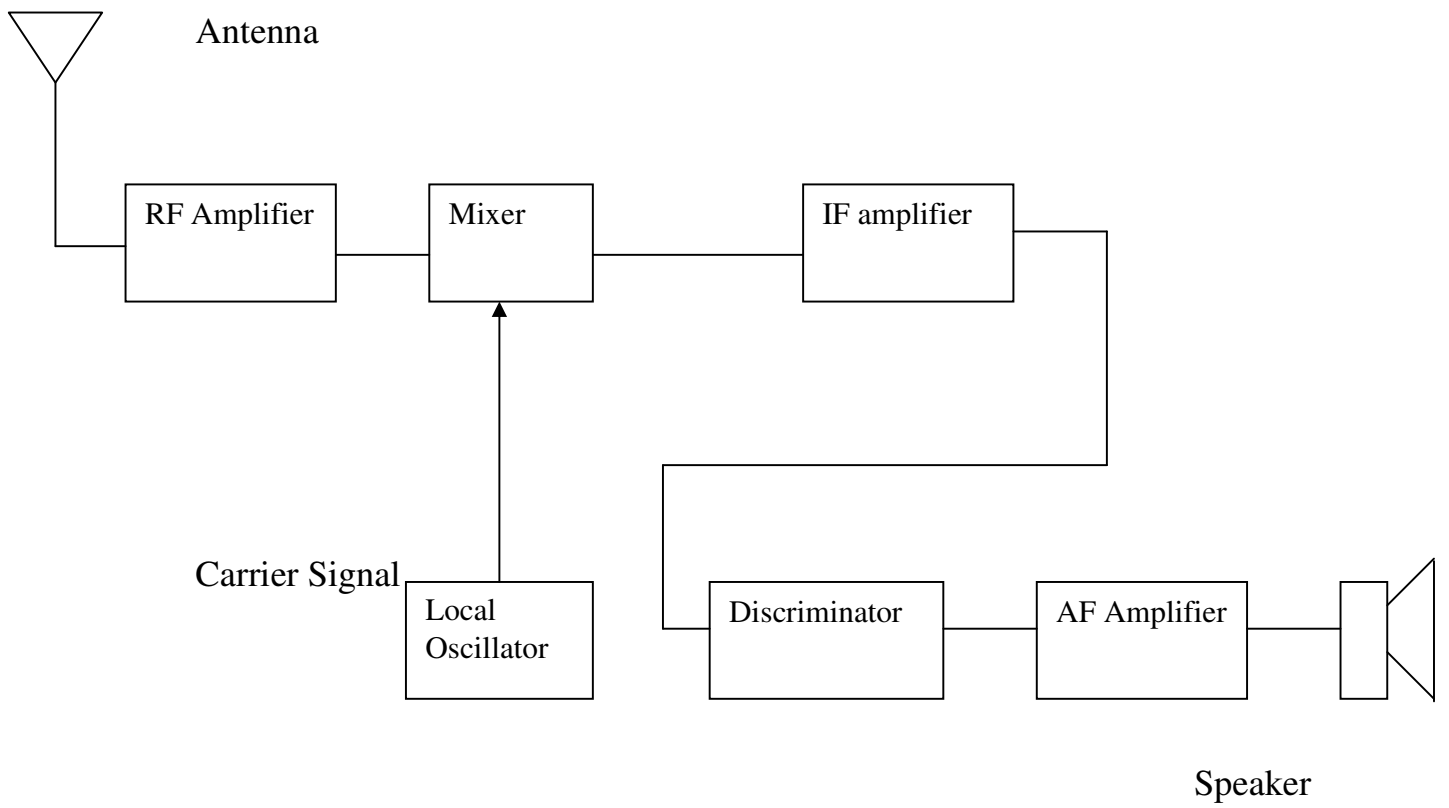
The frequency modulator circuit is constructed around a BF495, high frequency small signal BJT. The collector circuit of the transistor consists of a tank circuit formed by an inductor and capacitor. This tank circuit together with the transistor acts as an oscillator and produces the carrier frequency. The transistor circuit appears to the oscillator as a variable capacitance. This capacitance adds to the capacitance of the oscillator-tuned circuit.

The size of this capacitance depends on the change in the collector current which occurs for a given change in base voltage and this is determined by the Trans conductance of the transistor. The transistor transconductance depends on the bias voltage applied to the transistor base. The larger the bias voltage, the larger the value of  $g_m$  and the larger the value of  $g_m$  and the larger capacitance which is added to the capacitance of the oscillator tuned circuit consequently the transistor circuit behaves as a voltage variable capacitance. The bias voltage applied to the transistor base determines the overall capacitance seen by the oscillator and hence the frequency of the carrier. This resulting in FM signal

### **TELESCOPIC WHIP ANTENNA:**

A telescopic whip antenna is used to radiate the AM signal generated by the amplitude modulator.

### FM RECEIVER



## **HARDWARE DESCRIPTION OF FM RECEIVER TRAINER**

The Fm receiver trainer VCT-13 has the following sections

- 1.FM super heterodyne receiver
- 2.Buffer and filter
- 3.Audio power amplifier

### **FM SUPER HETERODYNE RECEIVER:**

The FM receiver is built with the dedicated FM receiver IC-CXA1619IC consists of the following sections namely RF amplifier, Mixer and oscillator, IF amplifier and quadrature detector .The circuit details and the description of IC-CXA1619IC are given in appendix

### **BUFFER AND FILTER:**

A buffer is used to prevent any loading to the previous stage .The filter section consists of a BPF with a Pass band to 20KHZ –15MHZ.A notch filter is also included to eliminate the 50Hz power supply noise

### **AUDIO POWER AMPLIFIER:**

The Audio power amplifier is constructed using ICTBA810 to increase the power level of the demodulated message signal to the required level. The gain of this amplifier can be adjusted by the user by varying the pot meter POT-1.the maximum gain of this audio amplifier is 25.the amplified signal can be given to a loud signal which can be extremely plugged into the VCT-13 trainer

**TABULATION:**

Waveform	Amplitude (V)	Time Period (msec)	Frequency
Modulating Signal			
Demodulated signal			

**PROCEDURE:**

9. The circuit wiring is done as shown in diagram
10. A modulating signal input given to the Frequency modulator can also be given from an external function generator or an AFO
11. If an external signal source with every low voltage level is used then this signal can be amplified using the audio amplifier before connecting to the input of the FM modulator
12. Now increase the amplitude of the modulated signal to the required level.
13. The amplitude and the time duration of the modulating signal are observed using CRO.
14. The amplitude and time duration of the modulated signal are observed using a CRO and tabulated.
15. The final demodulated signal is viewed using a CRO Also the amplitude and time duration of the demodulated wave are noted down

**RESULT:**

The modulating signal is transmitted after frequency modulation using VCT-12 and the signal is received back after demodulation using VCT-13

## **DESIGN OF WIRELESS DATA MODEM**

**EXPT NO: 4**

**AIM:**

To communicate between two microprocessors using wireless data modems.

**APPARATUS REQUIRED:**

- 1.8085 microprocessor kit - 2
2. Wireless data modem – 2

**DESIGN:**

Baud rate calculation:

Baud rate \* Required baud rate input to 8251 = Required clock

$$16 * 300 = 4800$$

Therefore, Required clock input to 8251 = 4800 Hz

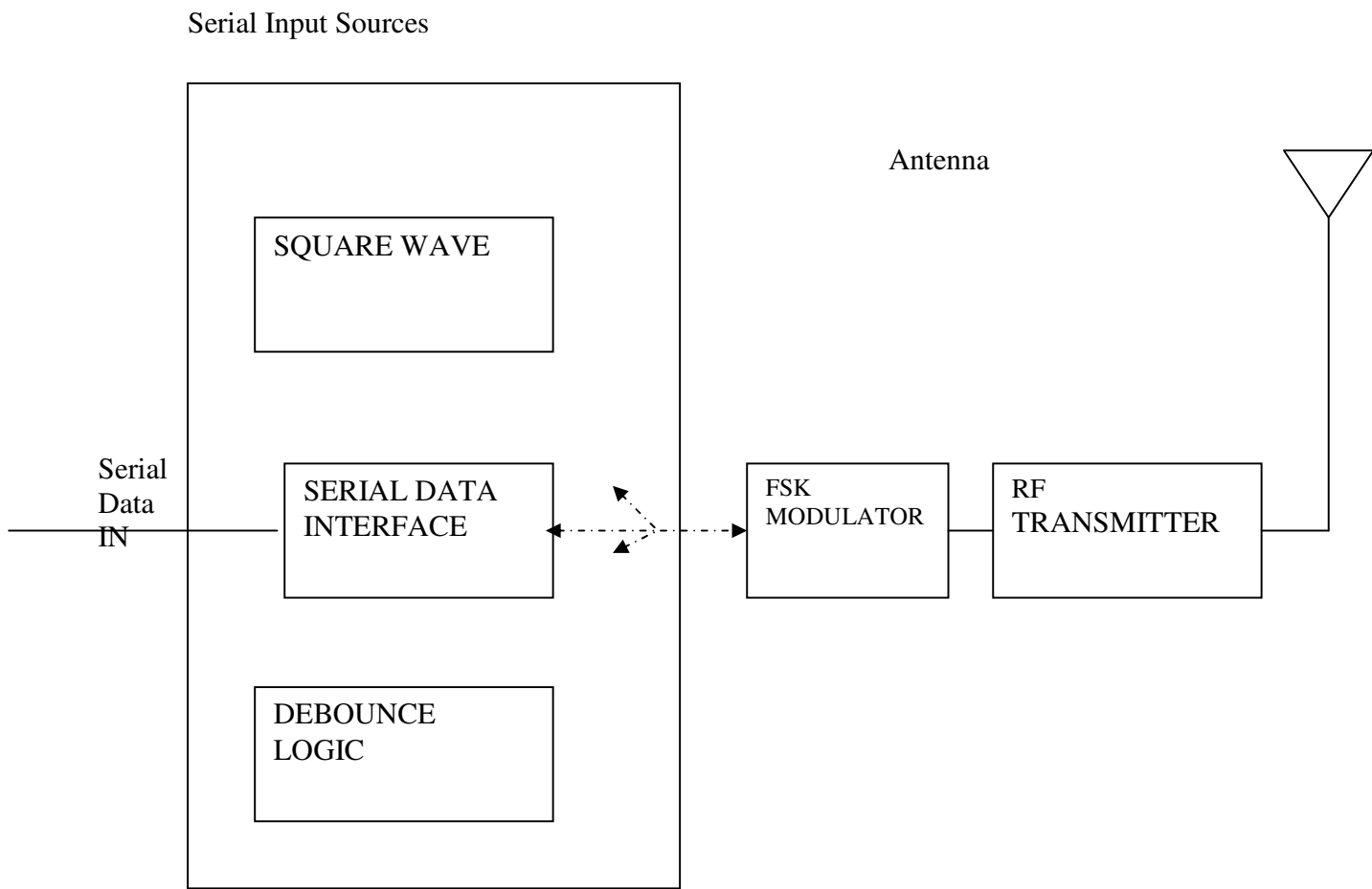
Count value = Clock input to 8253 / Required clock input to 8251

$$= 1.536 * 10^6 / 4800$$

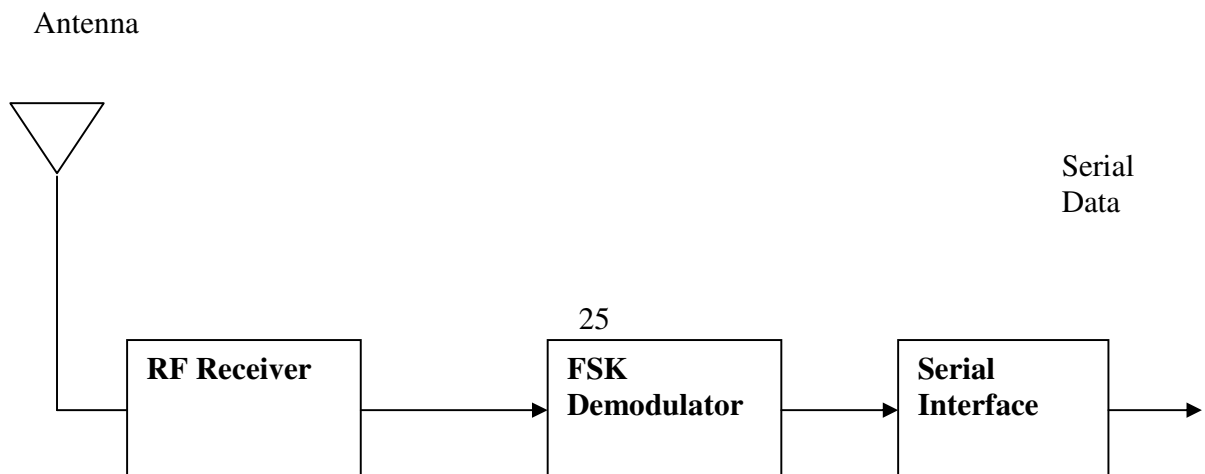
$$= 320 = 140 \text{ H.}$$



### HARDWARE DESCRIPTION OF VCT-10A



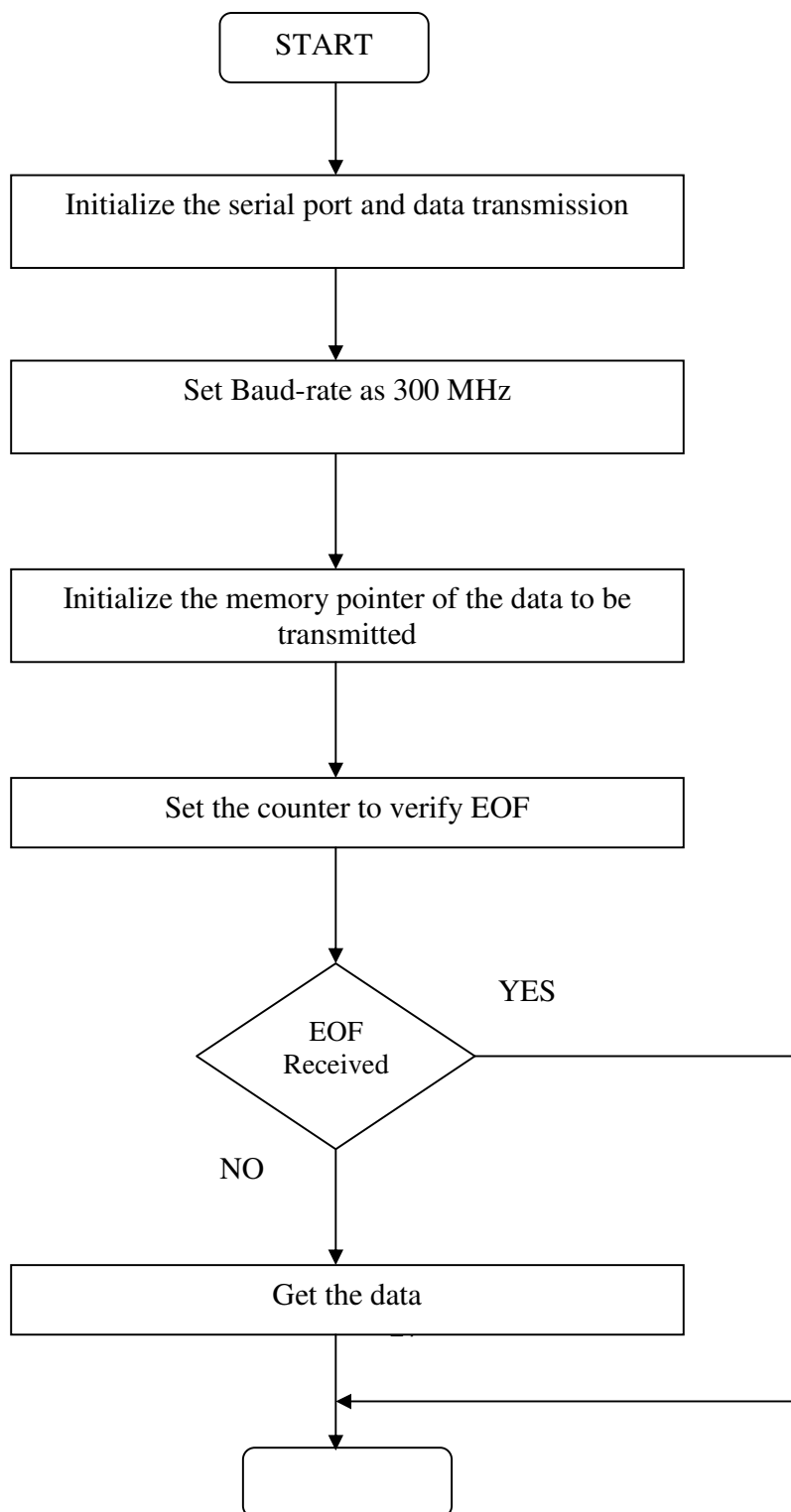
### HARDWARE DESCRIPTION OF VCT-10B



**ALGORITHM FOR TRANSMITTER:**

1. Initialize the serial port for data transmission.
2. Set baud rate as 300.
3. Initialize the memory pointer of the data to be transmitted.
4. Set a counter for verification of EOF.
5. Get the data from the consecutive memory locations and transmit it till EOF is reached.
6. Reset the system.

**FLOWCHART FOR TRANSMITTER**



**PROGRAM FOR TRANSMITTER:**

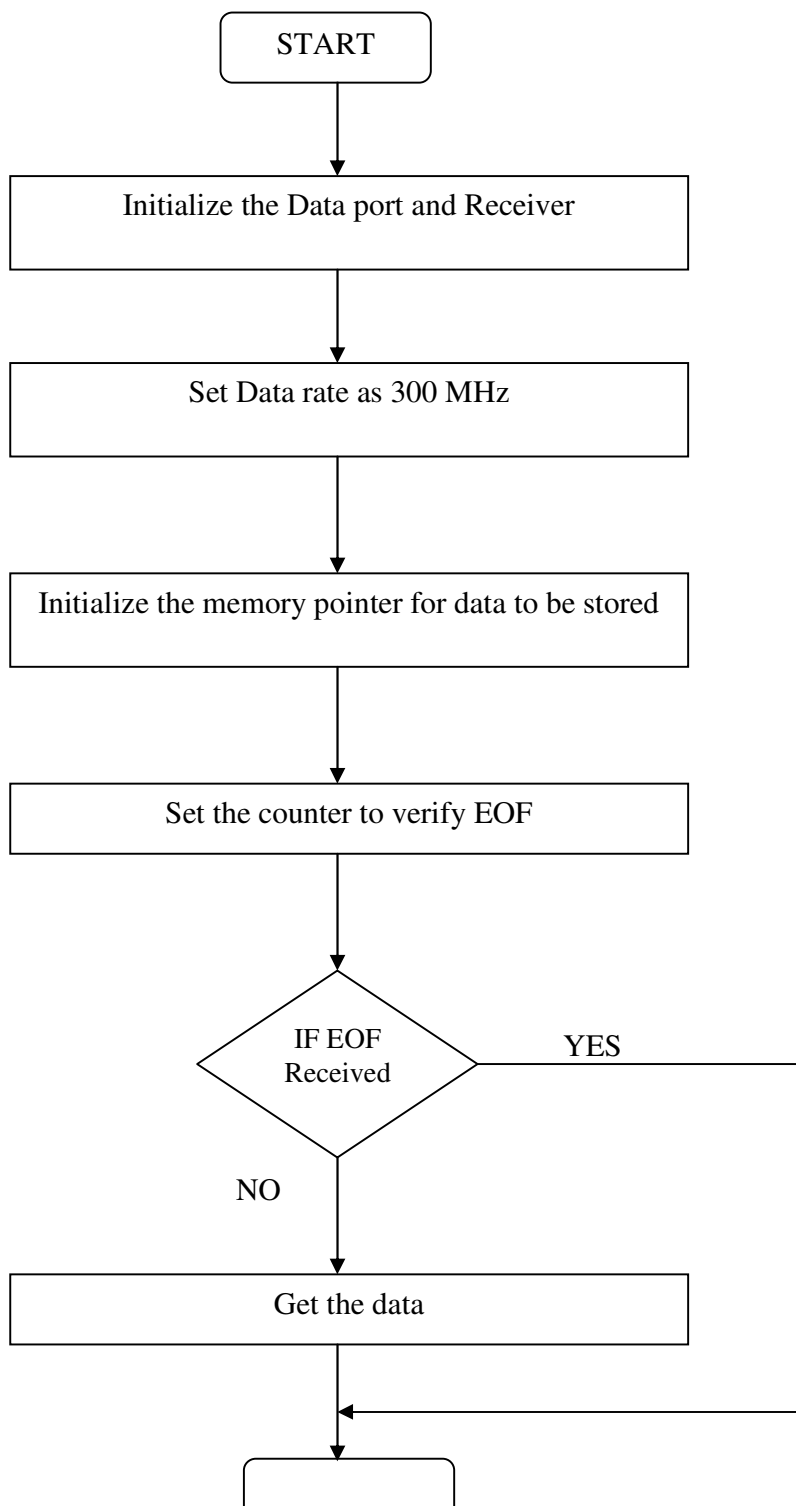
Address	Opcode	Label	Mnemonics	Operand	Comments
4100	21,00,45		LXI	H, 4500H	
4103	3E, 36		MVI	A, 36H	Set the timer
4105	D3, 0B		OUT	0BH	Channel 0 in mode 3
4107	3E, 40		MVI	A, 40H	Set baud rate as 300
4109	D3, 08		OUT	08H	
410B	3E, 01		MVI	A, 01H	
410D	D3, 08		OUT	08H	
410F	0E, 05	RELOAD	MVI	C, 05H	Load count
4111	DB, 05	CHECK	IN	05H	
4113	E6, 04		ANI	04H	Check transmitter empty
4115	CA, 11, 41		JZ	CHECK	
4118	7E		MOV	A, M	
4119	D3, 04 OUT		04H		
411B	23		INXH		
411C	FE, 3F		CPI	3FH	Check EOF
411E	C2, 0F, 41		JNZ	RELOAD	
4121	0D		DCR	C	

4122	C2, 11, 41		JNZ	CHECK			
4125	CF			RSTI			Reset

**ALGORITHM FOR RECEIVER:**

1. Initialize the serial port for data reception.
2. Set baud rate as 300.
3. Initialize the memory pointer for the data to be EOF.
4. Set a counter for verification of EOF.
5. Receive the data and store it in the consecutive memory locations till EOF is reached.
6. Reset the system.

### FLOWCHART FOR RECEIVER



PROGRAM FOR RECEIVER:

Address	Opcode	Label	Mnemonics	Operand	Comments
4100	21,00,45		LXI	H, 4500H	
4103	3E, 36		MVI	A, 36H	Set the timer
4105	D3, 0B		OUT	0BH	Channel 0 in mode 3
4107	3E, 40		MVI	A, 40H	Set baud rate as 300
4109	D3, 08		OUT	08H	
410B	3E, 01		MVI	A,01H	
410D	D3,08		OUT	08H	
410F	0E, 05	RELOAD	MVI	C, 05H	Load count
4111	DB, 05	CHECK	IN	05H	Check receiver is ready
4113	E6, 02		ANI 02		
4115	CA, 11, 41		JZ	CHECK	
4118	DB, 04 IN		04H		
411A	77		MOV	M, A	
411B	23		INX	H	
411C	D3, 04		CPI	3FH	Check EOF
411E	23		JNZ	RELOAD	

4121	FE, 3F	DCR	C	
4122	0D	JNZ	CHECK	
4125	CF	RSTI		Reset

**TABULATION:**

TRANSMITTER		RECEIVER	
ADDRESS	INPUT	ADDRESS	OUTPUT

**RESULT:**

Thus the communication between two microprocessors is made using wireless data modem.



## **PCB LAYOUT DESIGN USING CAD**

### **EXPT NO: 5**

#### **AIM:**

To design a printed circuit board layout for a given circuit.

#### **APPARATUS REQUIRED:**

1. Personal computer with windows os.
2. PCB layout software such as ORCAD.

#### **THEORY:**

General rules for designing PCBs:

The PCB designer follows few rules of thumb that can be used when laying out PCBs. Here they are,

#### **1.PLACING COMPONENTS:**

Generally, it is best to place parts only on the topside of the board. Firstly place all the components in specific locations. This includes connectors, switches, LED mounting holes, heat sinks or any other item that mounts to an external location.

Give careful thought when placing components to minimize trace lengths. Doing a good job here will make laying the traces much easier.

Arrange ICs in only one or two orientations (up and down or right and left). Align each IC so that pin 1 is in the same place for each orientation, usually on the top or left sides. Position polarized parts with the positive leads, all having the same orientation. Also use a square pad to mark the positive leads of these components.

Frequently, the beginners run out of room when routing traces. Leave 0.35 to 0.5 between ICs. For large ICs allow even more space.

Parts not found in the component library can be made by placing a series of individual pads and then group them together. Place one pad for each lead of the component. It is very important to measure the pin spacing and pin diameters as accurately as possible.

After placing all the components, print out a copy of the layout. Place each component on the top of the layout. Check to insure that you have allowed enough space for every part to rest without touching each other.

## 2.PLACING POWER AND GROUND TRACES:

After the components are placed, the next step is to lay the power and ground traces. A power rail is run along the front edge of the board and a ground rail along the rear edge. From these rails attach traces that run in between the ICs. The ground rail should be very wide, 0.100" and all the supply lines should be 0.50". When using this configuration the remaining of the bottom layer is then reserved for the vertical signal traces.

## 3.PLACING SIGNAL TRACES:

When placing traces, it is always a good practice to make them as short and direct as possible. Use vias to move signals from one layer to the other. A via is a pad-through hole. Generally the best strategy is to lay out a board with vertical trace on one side and horizontal traces on the opposite side. A good trace width for low current digital and analog signals is 0.010".

Traces that carry significant current should be wider than signal traces. The table below gives rough guidelines of how wide should a trace be for a given amount of current.

0.010"	0.3 Amps
0.015"	0.4 Amps
0.020"	0.7 Amps
0.025"	1 Amps
0.050"	2 Amps
0.100"	4 Amps
0.150"	6 Amps

When routing traces, it is best to have the snap to grid turned on. Setting the snap grid spacing to 0.050" works well. Changing to a value of 0.025" can be helpful when trying to work as densely as possible. Turning off the snap feature may be necessary when connecting to parts that have unusual pin spacing.

It is a common practice to restrict the direction that traces run to horizontal, vertical or at 45 degrees angles.

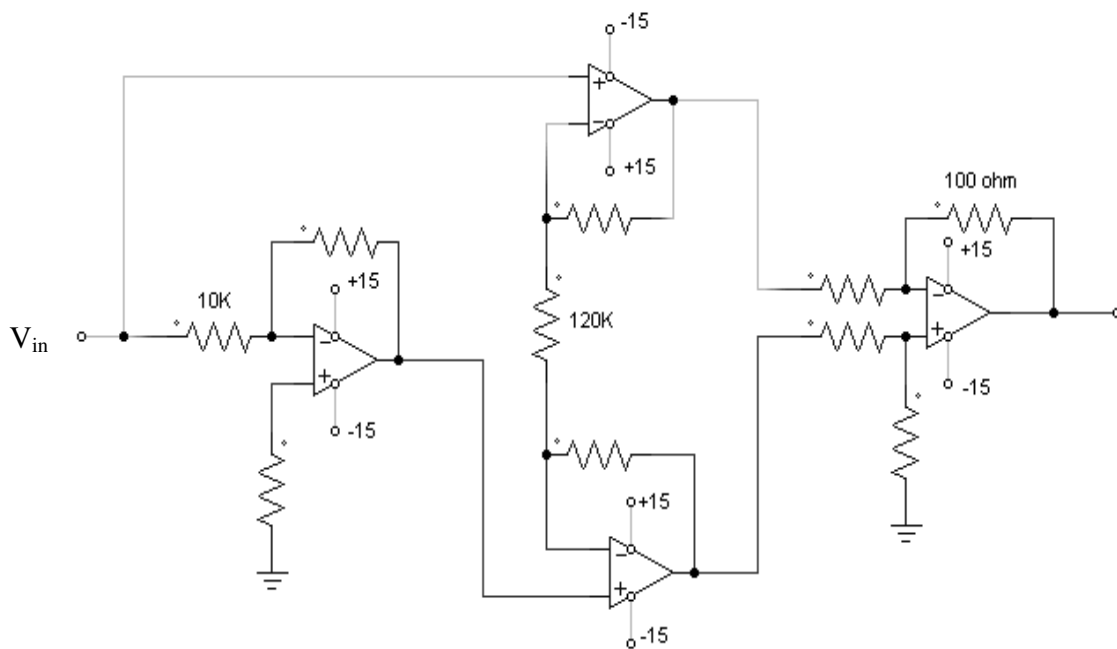
When placing narrow traces, use 0.015" or less. Avoid sharp right angle turns. The problem here is that, in the board manufacturing process the outside corner can be etched a little more narrow. The solution is to use two 45-degree bends with a short leg in between.

It is a good idea to place text on the top layer of the board, such as the product or company name.

#### 4.CHECKING YOUR WORK:

After all the traces are placed, it is best to double-check the routing of every signal to verify that nothing is missing or incorrectly wired. Do this by running through the schematic, one wire at a time. Carefully follow the path of each trace. After each trace is confirmed, mark the signal on the schematic with a yellow highlighter.

#### CIRCUIT DIAGRAM:



Inspect the layout, both top and bottom to ensure that the gap between every item is 0.007” or greater. Use the pad information tool to determine the diameters of pads that make up a component.

Check for missing vias. The CAD software will automatically insert a via when changing layers as a series of traces are placed. The user often forget that vias are not automatically inserted otherwise. For example, when beginning a new trace, a via is to first print a top layer , then print the bottom. Visually inspect each side for traces that doesn't connect to anything. When a missing via is found, insert one. Do this by clicking on the pad in the side tool bar from the down list box and click on the layout.

Check for the traces that cross each other. Inspecting a printout of each layer easily does this.

Metal components such as heat sinks, crystals, switches, batteries and connectors can cause shorts, if they are placed over traces on the top layer. Inspect for these shorts by placing all the metal components on a printout of the top layer. Then look for traces that run below the metal components.

**RESULT:**

Thus the PCB is designed using CAD.

## **DESIGN OF DC VOLTAGE REGULATOR USING SCR**

**EXPT NO: 6**

**AIM:**

To study the operation of DC voltage regulator with R load and observe the waveform.

**APPARATUS REQUIRED:**

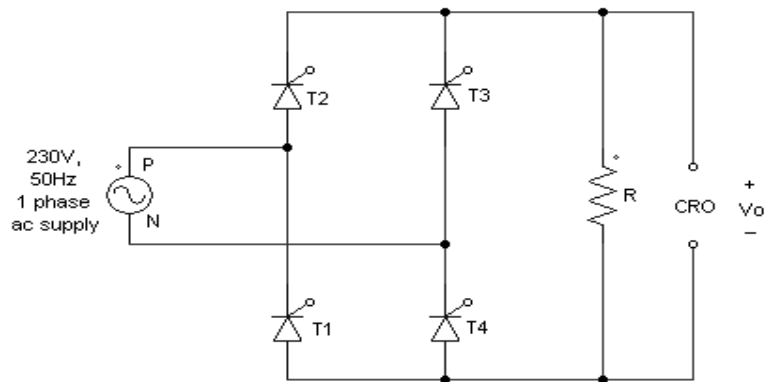
1. Single Phase SCR bridge converter trainer kit.
2. Patch chords.
3. CRO

**THEORY:**

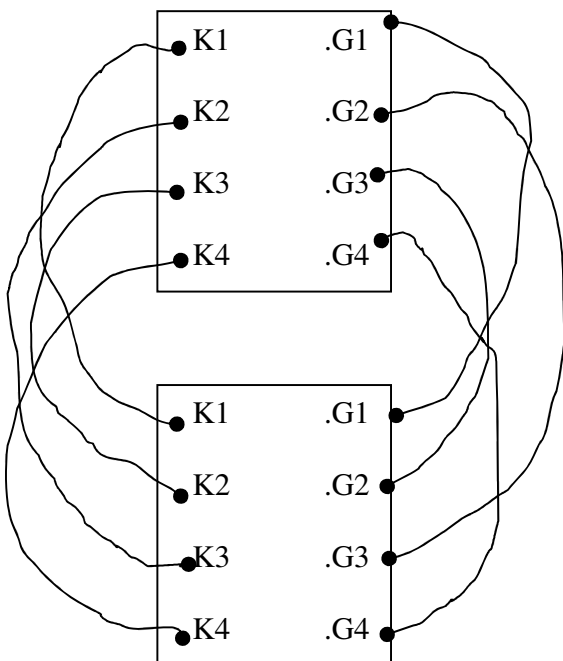
Rectification is a process of converting an AC to DC. The fully controlled converter uses thyristors as the rectifying elements and the Dc output as function of amplitude of the Ac supply voltage and the point at which the thyristors are triggered. During the positive half cycle of the input voltage SCR 1, SCR 2, are forward biased and are simultaneously triggered at the firing angle  $\alpha$ . The supply voltage appears across the load resistance R. The load voltage is 0 from  $\pi$  to  $\pi+\alpha$ , until the SCR 3 and SCR 4 are triggered in negative half cycle. The load current now flows from the supply, SCR 3, Load and SCR 4. thus the direction of current through the load is the same in both half cycles. The output voltage is given by the expression.

$$V_0 = V_m / \pi (1 + \cos\alpha) \text{ volts}$$

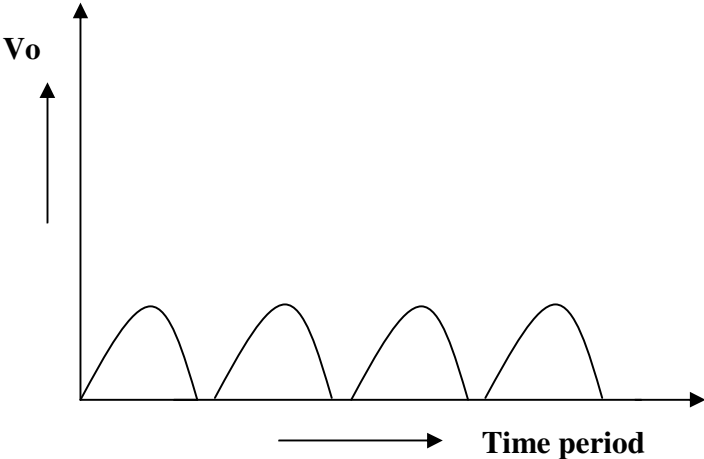
**CIRCUIT DIAGRAM:**



**TRIGGERING PULSE CIRCUIT :**

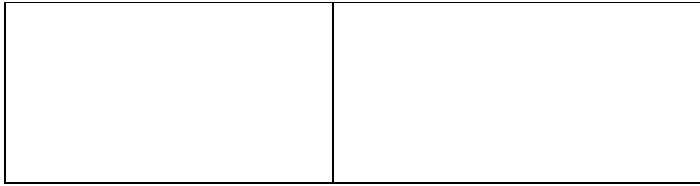


**MODEL GRAPH :**



**TABULATION:**

Firing Angle ( $\alpha$ )	Output DC voltage (volts)



**PROCEDURE:**

1. Switch ON the trainer power ON/OFF switch.
2. Switch ON the 24-volt AC power supply.
3. Switch ON the debounce logic switch and connect the R load.
4. Vary the controlled voltage from minimum to maximum.
5. For each step note down the Firing angle and the output voltage.

**RESULT:**

Thus the operation of fully controlled converter with R load has been studied and the waveforms are observed.



## **MICROCONTROLLER BASED SYSTEM DESIGN**

**EXPT NO: 7**

**AIM:**

To interface a stepper motor with 8051 micro controller and operate it.

**APPARATUS REQUIRED:**

1. 8051 micro controller kit
2. Stepper motor
3. Interface card

**THEORY:**

A motor in which the rotor is able to assume only discrete stationary angular position is a stepper motor. They are used in printer, disk drive process control machine tools etc.

Two-phase stepper motor has two pairs of stator poles. Stepper motor windings A1, A2, B1, B2 are cyclically excited with a DC current to run the motor in clockwise direction and reverse phase sequence A1, B2, A2, B1 in anticlockwise stepping

Two-phase switching scheme:

In this scheme, any two adjacent stator windings are energized.

Anticlockwise						Clockwise					
Step	A1	A2	B1	B2	Data	Step	A1	A2	B1	B2	Data
1	1	0	0	1	9 H	1	1	0	1	0	A H
2	0	1	0	1	5 H	2	0	1	1	0	6 H
3	0	1	1	0	6 H	3	0	1	0	1	5 H
4	1	0	1	0	A H	4	1	0	0	1	9 H

Address Decoding logic:

The 74138 chip is used for generating the address decoding logic to generate the device select pulses CS1 and CS2 for selecting the IC 74175 in which latches the data bus to stepper motor driving circuitry.

**PROGRAM:**

Address	Opcode	Label	Mnemonics	Operand	Comments
4100	90 41 1F	START	MOV	DPTR # TABLE	Load the start address of switching scheme data TABLE into Data pointer.
4103	78 04		MOV	R0, #04	Load the count in R0
4105	F0	LOOP	MOV X	A, @ DPTR	Load the number in TABLE into A
4106	C0 83		PUSH	DPH	Push DPTR Value to stack
4108	C0 82		PUSH	DPL	
410A	90 FF C0		MOV	DPTR, # 0FFFC0	Load the motor port address into DPTR.
410D	F0		MOV X	@ DPTR, A	Send the value in A to stepper motor port address
410F	7C FF		MOV	R4,#0FFH	Delay loop to cause a specific amount of time delay before next data item is sent to the motor
4110	7D FF	DELAY	MOV	R5,#0FFH	
4112	DD FE	DELAY1	DNZ	R4, DELAY 1	
4114	DC FA		DJNZ	R4,DELAY	
4116	D0 82		POP	DPL	POP back DPTR value from stack
4118	D0 83		POP	DPH	
411A	A3		INC	DPTR	Increment DPTR to point to next item in

					the TABLE
411B	D8 E8		DJNZ	R0, LOOP	Decrement R0, if not zero repeat the loop
411D	80 E1		SJMP	START	Short jump to start of the program to make the motor rotate continuously.
411F	09 05 06 0AH	TABLE	DB	09 05 06 0AH	Value as per two phase switching scheme.

**RESULT:**

Enter the above program starting from location 4100 and execute the same, stepper motor rotates. Varying the count at R4 and R5 can vary the speed. Entering the data in the look-up TABLE in the reverse order can vary the direction of rotation.

## DESIGN OF PROCESS CONTROL TIMER

**EXPT NO: 8**

**AIM:**

To design an process control timer using relay.

**APPARATUS REQUIRED:**

1. Transistor – CL100 –2 no.s
2. Relay – 1
3. Diode – IN4001 – 1
4. LED – 1
5. Capacitor – 100  $\mu$ F-1
6. Resistor- 4.7K $\Omega$ . 2.2 K $\Omega$ .
7. Regulated Power supply

**DESIGN:**

$$V_C = V_{CC} (1 - e^{-t/RC}) \text{-----(1)}$$

Where R = 4.7 K $\Omega$ .

C = 100  $\mu$ F

Let the operation voltage be  $V_{opr}$ . At  $t = T$ , voltage across the capacitor is equal to the sum of the relays operating voltage and the two diode drops of Darlington pair.

The calculation of T is given as follows

$$V_C = V_{CC}$$
$$C_1 = e^{-t/RC}$$

From equation (1) at  $t = 0$ ,  $V_C = 0$  and at  $t = \infty$ ,  $V_C = V_{CC}$

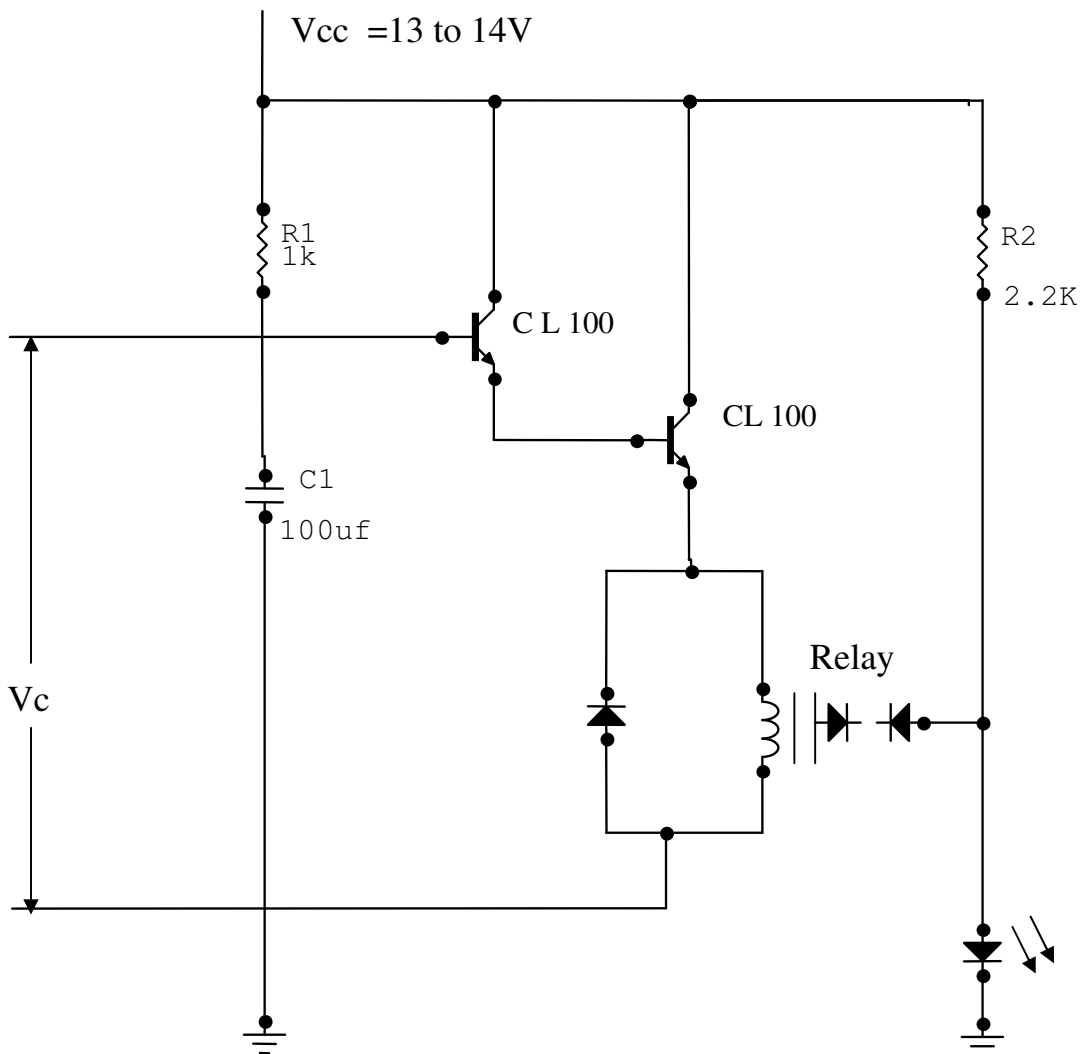
$$V_O = V_{CC} (1 - e^{-t/RC}), V_{CC} = 13V$$
$$= 13(1 - e^{-t/RC})$$

R = 4.7 K $\Omega$ .      C = 100  $\mu$ F

$$7.97 = 13 (1 - e^{-t/(4.7K\Omega * 100\mu F)}) \text{ and } t = 6 \text{ sec.}$$

Which is the theoretical value of time period for switching from one device to another.

**CIRCUIT DIAGRAM :**



### **THEORY:**

The analog timer circuit shown in the diagram consists of darlington pair and relay circuit connected with proper biasing. The relay circuit is designed to operate at operating voltage  $V_{opr}$  which is given by

$$V_{opr} = V_{CC} (1 - e^{-t/RC}) + 2 \text{ diode drops}$$

Where  $V_{CC}$  – supply voltage  
t – time period

R and C are the values of biasing resistor and capacitor. Also  $V_C = V_{CC} (1 - e^{-t/RC})$

When the supply voltage  $V_{CC}$  (ranging from 13 to 14V) is given to the circuit, device A is turned ON. The current flowing through the circuit charges the biasing capacitor upto a voltage equal to sum of relay operating voltage and the two diode drop of this voltage is reached. Once this relay lead the switch positions the time taken by the analog timer to switch from one device to another is calculated, whose theoretical value is 6 sec.

### **PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. Now supply voltage of 13V is given and time taken by the relay to switch from one device A to device B (i.e) time taken to switch ON the LED is noted.

### **RESULT:**

Thus the analog timer was designed using relay.

Theoretical value of time taken = -----

Practical value of time taken = -----

## DESIGN OF INSTRUMENTATION AMPLIFIER

**EXPT NO: 9**

**AIM :**

To construct an Instrumentation amplifier using LF356 for a gain of 250, which amplifies the voltage of thermocouple circuit.

**APPARATUS REQUIRED:**

1. Instrumentation amplifier
2. Regulated power supply.
3. Thermocouple
4. CRO

**DESIGN :**

Consider fig(i)

At node 1:

$$\begin{aligned}V_{O1}-V_1/R_2 + (V_2-V_1)/R_1 &= 0 \\R_1 * V_{O1} + R_2 * V_2 - V_1(R_1+R_2) &= 0 \\V_{O1} &= V_1(1+R_2/R_1) - V_2 * R_2/R_1 \text{-----(1)}\end{aligned}$$

At node 2:

$$\begin{aligned}V_{O2}-V_2/R_2 + (V_1-V_2)/R_1 &= 0 \\R_1 * V_{O2} + R_2 * V_1 - V_2(R_1+R_2) &= 0 \\V_{O2} &= V_2(1+R_2/R_1) - V_1 * R_2/R_1 \text{-----(2)}\end{aligned}$$

Output voltage of the instrumentation amplifier,

$$V_{out} = (V_{O2} - V_{O1}) * (R_3/R) \text{-----(3)}$$

Substituting for  $V_{O2}$  &  $V_{O1}$  from equations (1),(2) and (3)

$$V_{out} = [V_2(1+R_2/R_1) - V_1 * R_2/R_1 - V_1(1+R_2/R_1) + V_2 * R_2/R_1] * (R_3/R)$$

As  $\Delta V = V_2 - V_1$ , therefore

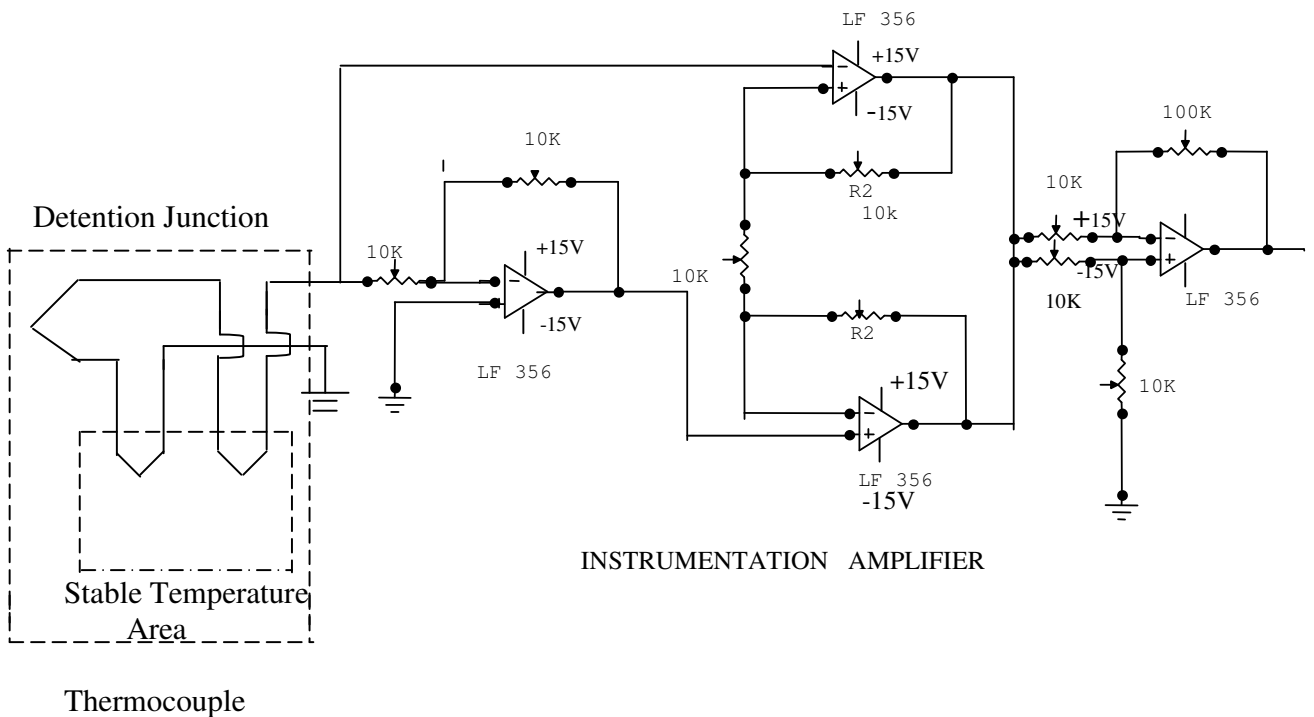
$$\underline{V_{out} / \Delta V} = R_3 / R(1 + 2 * R_2 / R_1)$$

This is gain equation for instrumentation amplifier.  
 $R_3 / R$  is assumed to be 10 by choosing  $R_3 = 100\text{ K}\Omega$ ,  $R = 10\text{ K}\Omega$ . The two  $R_3$ 's are matched for the same value. The two  $R_2$ 's are matched using  $120\text{ K}\Omega$  resistances and the  $R_1$  value is chosen to be  $10\text{ K}\Omega$  and thus the gain obtained is 250.

**THEORY:**

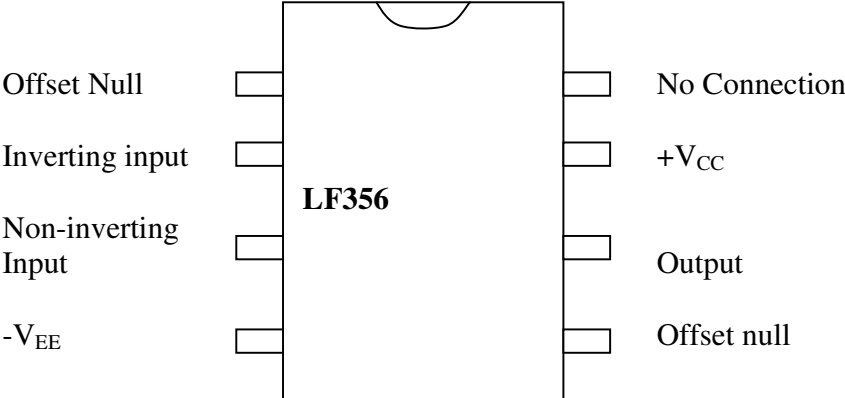
In a number of industrial and consumer applications physical quantities such as temperature, pressure, light intensity are to be measured and controlled. These physical quantities are measured with the help of transducers has to be amplified so that it can drive the display system. This function is performed by an instrumentation amplifier

**CIRCUIT DIAGRAM :**





**PIN DIAGRAM OF LF356:**



The important features of instrumentation amplifier are:

1. High Gain Accuracy
2. High CMRR
3. High Gain Stability With Low Temperature Coefficient
4. Low Dc Output
5. High Output Impedance

**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. The voltage from the bridge type transducer part (thermocouple) is amplified by the instrumentation amplifier.
3. The amplified output voltage is noted for different temperature values.
4. A graph is plotted between the temperature and the amplified voltage.

**RESULT:**

Thus the instrumentation amplifier was designed and the graph is plotted.

## **DSP BASED DIGITAL FUNCTION GENERATOR**

**EXPT NO: 10**

**AIM:**

To stimulate a simple pulse generator using ADSP2181 DSP processor

**APPARATUS REQUIRED:**

1. ADSP2181 unit
2. ADSP 2181 Universal
3. CRO
4. IBM PC keyboard

**THEORY:**

ADSP 2181 is highly advanced DSP processor, which works of on chip serial port. It is capable of processing 16-bit arithmetic operation, with ALU and Accumulator. This ADSP2181 is suitable for developing applications like adaptive filtering, FET & external precision arithmetic etc., In this experiment a simple pulse generator is stimulated using ADSP2181.

In order to develop this application IBM PC keyboard is connected to ADSP2181 through the IO port of 0x02

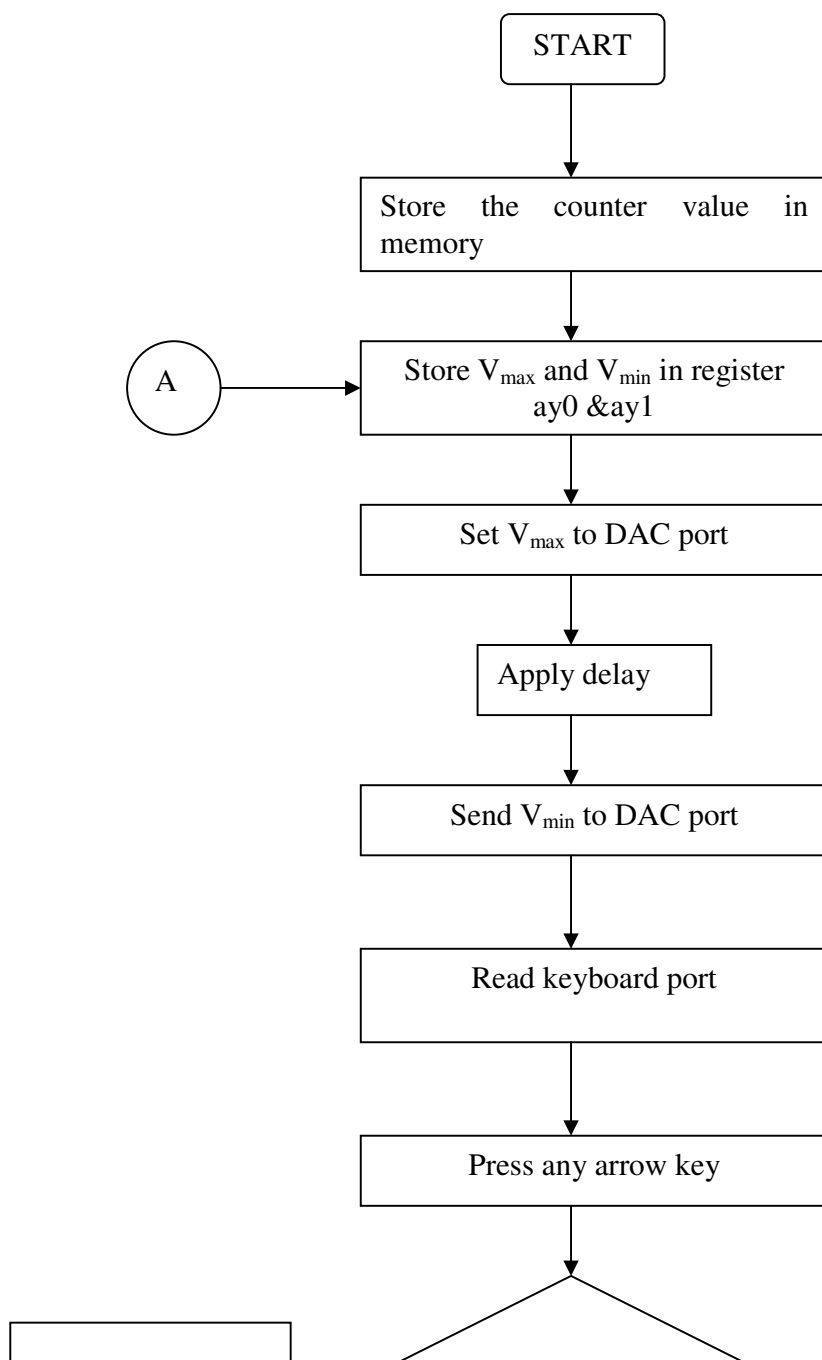
The IBM PC keyboard up arrow is used to increase the amplitude of the pulse wave, down arrow is used to decrease the amplitude, left arrow is used to decrease the frequency and right arrow is used to increase the frequency.

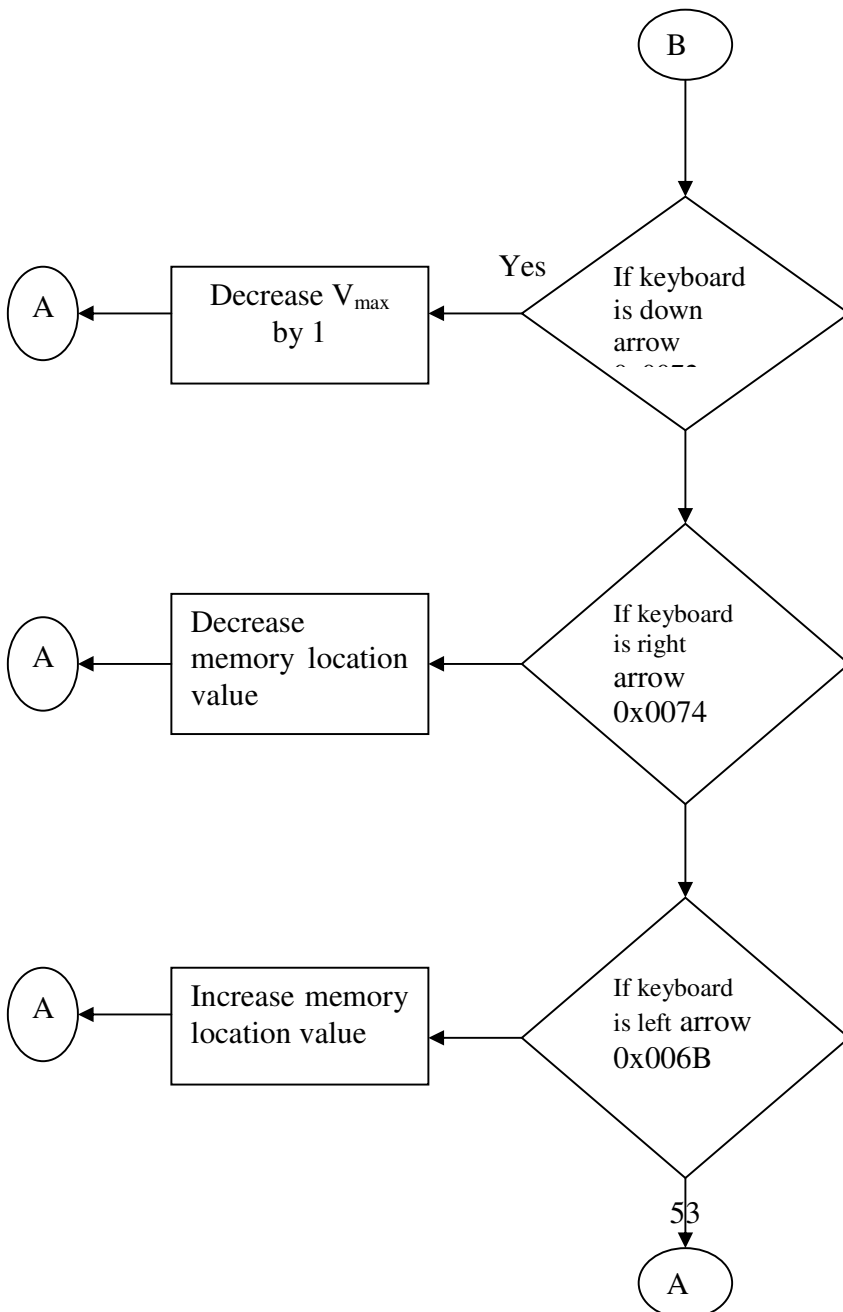
**PROBLEM STATEMENT:**

1. USING ADSP2181 generate the square wave and measure the amplitude of the square wave and frequency

2. Identify scan codes for the up arrow , down arrow, right and left arrow by reading the IO port through which IBM PC keyboard is connected to the IO port of ADSP2181
3. Find the suitable logic and wrote a program to increase and decrease the amplitude of square wave using CRO

### FLOWCHART





**SAMPLE PROGRAM:**

```
.module /ram main _routine;
start:
    ay0 =0xffff; [max peak voltage]
beg:
    cntr =0xffff; [delay counter]
    do int until ce;
    ax0 =0x0000;
int:
    io(0x14) =ay0;[send max peak to DAC]
    ax1=io(0x102);[read keyboard port]
    dm(0x103) =ax1; [store the scan cade for the pressed key]
    ay1 = 0x0ff; [max upper bytes]
    ar=ax1 and ay1;
    ax1=ar;
    ay1=0x0075;[scan code for up arrow key]
    ar=ax1-ay1 ; [do camparision]
    dm(0x105)=ar;
    if ne jump beg;[if not equal repeat the same square wave]
    ay =ay0+1;[if equal increase the max peak voltage repeat the square wave]
    ay0=ar;
    dm(0x106)=ay0;
    jump beg;
    idle;
.end mod;
```

**EXERCISE:**

In the given program pulse generator is stimulated only using up arrow key so the students instructed to stimulate the same using down arrow , left arrow & right arrow kkeys by identifying the key codes

**PROGRAM:**

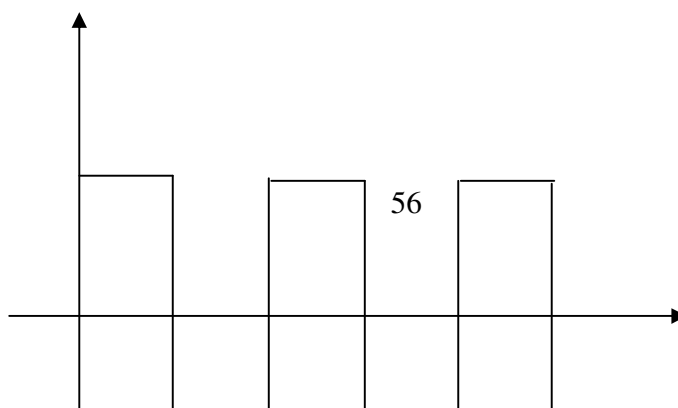
```
.module /ram main_routine;
start:
    ay0 =0xff;[max peak voltage]
    ax1 =0xff;
    dm(0x107)=ax1;
beg:   cntr =dm(0x107);[delay counter]
    do int until ce;
    ax0=0x0000;
int:   io(0x14) =ax0 ; [send minimum peak to DAC]
    cntr =dm(0x107);
    do ict until ce;
ict:   io(0x14)=ay0;[send maximum peak to DAC]
    ax1=io(0x102); [read keyboard port]
    dm(0x103)=ax1;[store scan code for pressed key]
    ay1=0x0ff;
    ar=ax1 and ay1;
    ax1 =ar;
    ay1=0x0075;[scan code for up arrow key]
    ar=ax1 -ay1;[do comparision]
    dm(0x105)=ar;
    if ne jump aaa;[if not equal check for another key]
    ar=ay0+1;[ increase amplitude]
    ay0=ar;
    dm(0x106)=ay0;
    jump beg;
aaa:   ay1=0x0072;[scan code for down arrow key]
    ar=ax1-ay1;[do comparision]
    dm(0x108)=ar;
    if ne jump bbb;[if not equal check for another key]
    ar=ay0-1;[ decrease amplitude]
    ay0=ar;
    dm(0x106)=ay0;
    jump beg;
bbb:   ay1=0x0072;[scan code for right arrow key]
    ar=ax1-ay1;[do comparision]
    dm(0x109)=ar;
    if ne jump ccc;[if not equal check for another key]
    ax1=dm(0x107)
    ar=ax1+5;[ decrease frequency]
    dm(0x107)=ar;
    jump beg;
ccc:   ay1=0x0074;[scan code for left arrow key]
    ar=ax1-ay1;[do comparision]
```

```
dm(0x110)=ar;
if ne jump beg;[if not equal check for another key]
ax1=dm(0x107)
ar=ax1-5;[ increase frequency]
dm(0x107)=ar;
jump beg;
idle;
.end mod;
```

**TABULATION COLUMN:**

	AMPLITUDE ( V )	TIME PERIOD (MS)	
SQUARE WAVE		T <sub>ON</sub>	T <sub>OFF</sub>

**MODEL GRAPH :**





↑  
V  
VOLTS  
↓

← T msec →

**RESULT:**

Thus the square wave is generated using ADSP2181 DSP.

## **SIMULATION OF DC VOLTAGE REGULATOR USING SCR**

**EXPT NO: 11**

**AIM:**

To study the operation of DC voltage regulator with R load and observe the waveform using MATLAB 6.5 software.

**APPARATUS REQUIRED:**

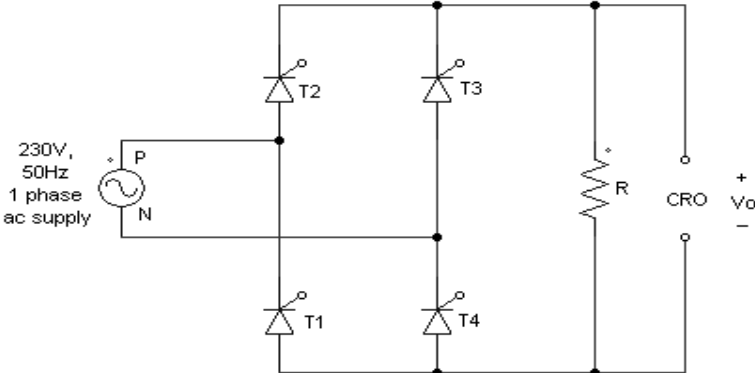
MATLAB 6.5 software

**THEORY:**

Rectification is a process of converting an AC to DC. The fully controlled converter uses thyristors as the rectifying elements and the Dc output as function of amplitude of the Ac supply voltage and the point at which the thyristors are triggered. During the positive half cycle of the input voltage SCR 1, SCR 2, are forward biased and are simultaneously triggered at the firing angle  $\alpha$ . The supply voltage appears across the load resistance R. The load voltage is 0 from  $\pi$  to  $\pi+\alpha$ , until the SCR 3 and SCR 4 are triggered in negative half cycle. The load current now flows from the supply, SCR 3, Load and SCR 4. thus the direction of current through the load is the same in both half cycles. The output voltage is given by the expression.

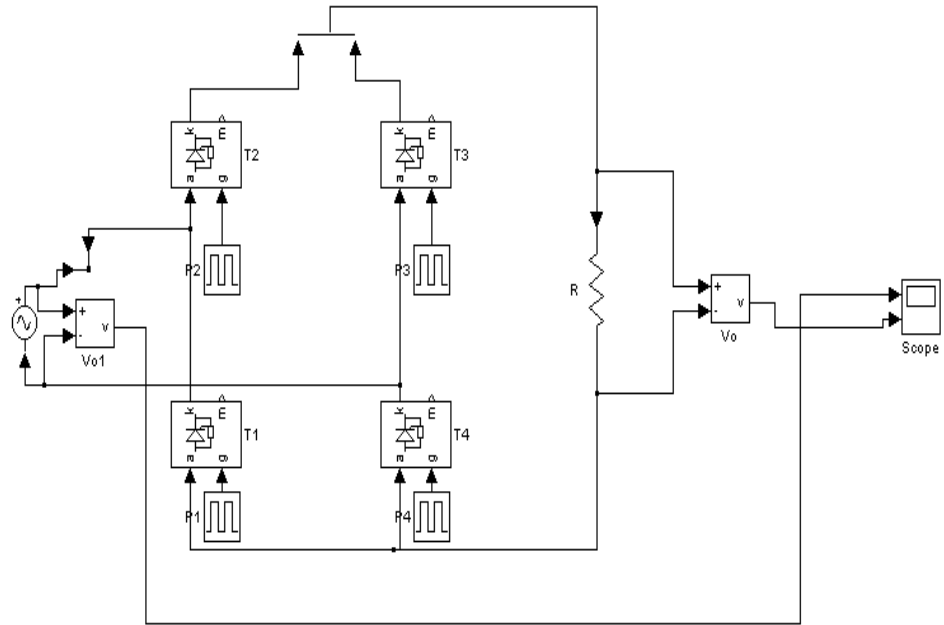
$$V_0 = V_m / \pi (1 + \cos\alpha) \text{ volts}$$

**CIRCUIT DIAGRAM:**



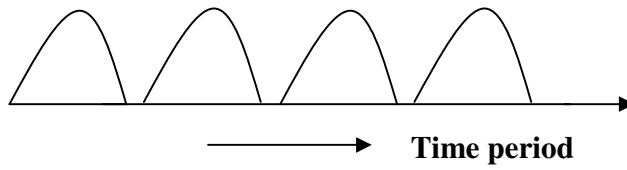
**PROCEDURE:**

1. Open the SIMULINK library from MATLAB 6.5.
2. Select the components from the blockset.
3. Give the wiring connection as per the circuit diagram.
4. Simulate the circuit and observe the waveform.



**MODEL GRAPH :**





**RESULT:**

Thus the operation of fully controlled converter with R load has been studied and the waveforms are observed.

**SIMULATION OF AC VOLTAGE CONTROLLER**  
**USING SCR**

**EXPT NO: 12**

**AIM:**

To study the operation of single phase AC voltage regulator with R load and observe the waveform using MATLAB 6.5 software.

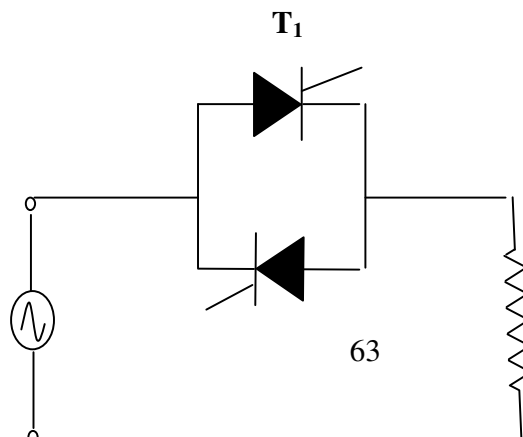
**APPARATUS REQUIRED:**

MATLAB 6.5 software

**THEORY:**

AC voltage controllers are thyristor-based devices, which convert the fixed alternating voltage directly to variable alternating voltage without a change in the frequency. The single phase AC voltage controller uses two thyristors connected in anti parallel. The thyristors T1 and T2 are forward biased during the positive and negative half cycles respectively. During the positive half cycle, T1 is triggered at firing angle  $\alpha$ . T1 starts conducting and the voltage source is applied to the load from  $\alpha$  to  $(\pi+\alpha)$ . During the negative half cycle T2 is triggered at  $(\pi+\alpha)$ , hence it conducts from  $(\pi+\alpha)$  to  $2\pi$ .

**CIRCUIT DIAGRAM:**

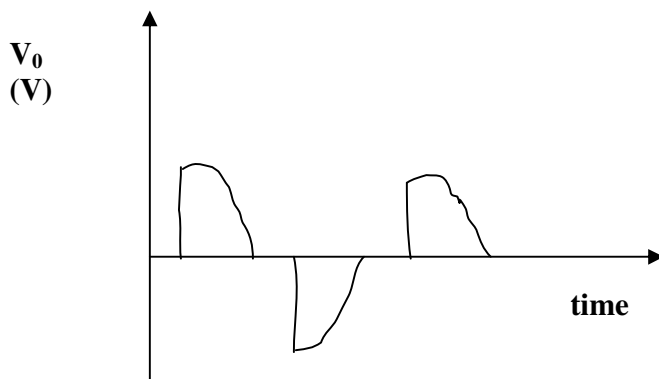


230V 50  
Hz, 1 $\phi$   
AC Supply

T<sub>2</sub>

R Load

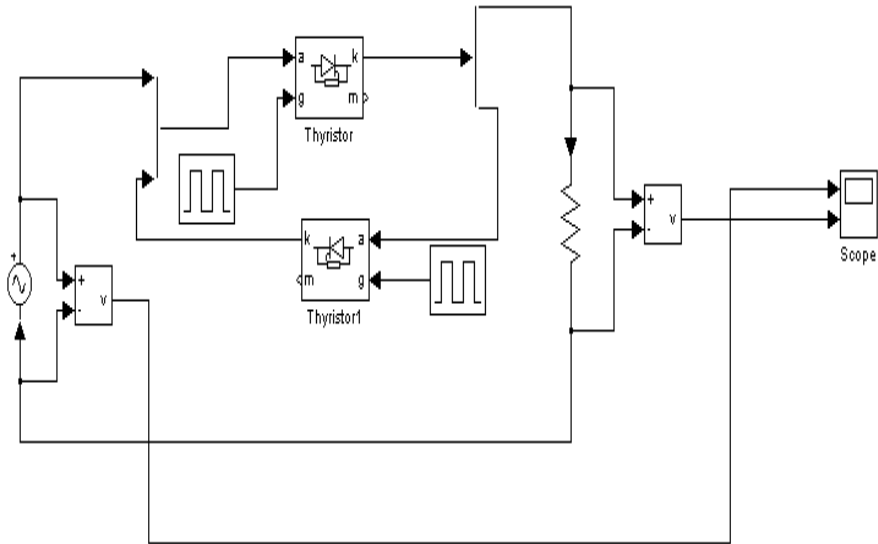
**MODEL GRAPH:**



**PROCEDURE:**

1. Open the SIMULINK library from MATLAB 6.5.
2. Select the components from the blockset.
3. Give the wiring connection as per the circuit diagram.
4. Simulate the circuit and observe the waveform.





**RESULT:**

Thus the operation of single phase AC voltage controller with R load has been studied and the waveforms are observed

