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10ES33

Third Semester B.E. Degree Examination, Dec. 2013/Jan. 2014
Logic Design

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions, selecting
atleast TWO questions from each part.**

PART – A

1.
 - a. Design a three –input, one – output minimal tow-level gate combinational circuit which has an output equal to 1 when majority of its inputs are at logic 1 and has an output equal to 0 when majority of its inputs are at logic 0. (08 Marks)
 - b. Minimize the expression :

$$\bar{Y} = \bar{A} B \bar{C} \bar{D} + \bar{A} B C \bar{D} + A B \bar{C} \bar{D} + A B C \bar{D} + A \bar{B} \bar{C} D + \bar{A} \bar{B} C \bar{D}.$$
 (06 Marks)
 - c. Reduce the following function using K – Map technique
 $f(A, B, C, D) = \pi M(0, 3, 4, 7, 8, 10, 12, 14) + d(2, 6).$ (06 Marks)
2.
 - a. Obtain all the prime implicants of the following Boolean function using Quine – McCluskey method.
 $f(a, b, c, d) = \Sigma(0, 2, 3, 5, 8, 10, 11)$
 verify the result using k – Map technique. (10 Marks)
 - b. Simplify the given function using MEV technique taking the least significant variable as the map entered variable
 $f(a, b, c, d, e) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14, 17, 19, 20, 22, 25, 27, 28, 30) + \Sigma d(8, 10, 24, 26).$ (10 Marks)
3.
 - a. Implement the multiple functions :
 $f_1(a, b, c, d) = \Sigma(0, 4, 8, 10, 14, 15)$ and
 $f_2(a, b, c, d) = \Sigma(3, 7, 9, 13)$ using two 3 to 8 decoders. (06 Marks)
 - b. Implement the following with a suitable decoder with active to enable input and active high output :
 $f(w, x, y, z) = \Sigma(3, 7, 9)$
 $g(a, b, c) = \pi(2, 4, 7).$ (08 Marks)
 - c. Draw the interfacing diagram of ten key keypad interface to a digital system using decimal to BCD encoder. (06 Marks)
4.
 - a. Configure a 16 to 1 MUX using 4 to 1 MUX. (06 Marks)
 - b. Implement the following Boolean function with 8 : 1 multiplexer
 $f(A, B, C, D) = \Sigma_m(0, 2, 6, 10, 11, 12, 13) + d(3, 8, 14).$ (06 Marks)
 - c. Write a truth table for two – bit magnitude comparator. Write the K – Map for each output of two – bit magnitude comparator and the resulting equation. (08 Marks)

PART – B

5.
 - a. What do you mean by sequential circuit? Explain with the help of block diagram? (04 Marks)
 - b. Explain with timing diagram, the working of SR latch as a switch debouncer. (06 Marks)
 - c. Explain the working of a master – slave JK flip-flop with the help of logic diagram, function table, logic symbol and timing diagram. (10 Marks)

- 6 a. Obtain the characteristic equation for a SR flip-flop. (04 Marks)
 b. Design a 4-bit register using positive edge triggered D flip-flops to operate as indicated in the table below : (08 Marks)

Mode select		Register operation
a_1	a_0	
0	0	Hold
0	1	Synchronous clear
1	0	Complement contents
1	1	Circular shift right

- c. Design a synchronous Mod - 6 counter using JK flip - flop. (08 Marks)
- 7 a. Explain mealy and Moore models of a clocked synchronous sequential circuits. (08 Marks)
 b. Analyse the synchronous sequential circuit shown in Fig. Q7(b). (12 Marks)

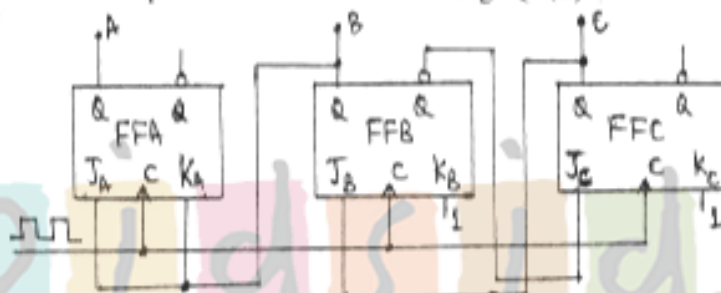


Fig. Q7(b)

- 8 a. Write the basic recommended steps for design of a clocked synchronous sequential circuit. (06 Marks)
 b. Construct the excitation table, transition table, state table and state diagram for the Moore sequential circuit shown in Fig. Q8(b). (14 Marks)

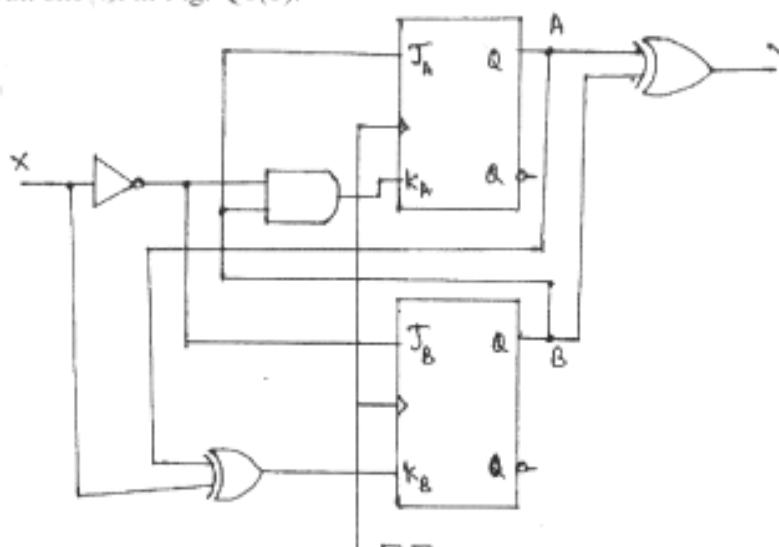


Fig. Q8(b)
